DIRECT DYNAMIC CONTROL OF IMPEDANCE FOR VAR AND HARMONIC COMPENSATION

A Thesis
Presented to
The Academic Faculty

by

Anish Prasai

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in
Electrical Engineering

School of Electrical and Computer Engineering
Georgia Institute of Technology
December 2011

DIRECT DYNAMIC CONTROL OF IMPEDANCE FOR VAR AND HARMONIC COMPENSATION

Approved by:

Professor Deepak M. Divan, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor David G. Taylor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Ronald G. Harley
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor J. Rhett Mayor
School of Mechanical Engineering
Georgia Institute of Technology

Professor Thomas G. Habetler
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: October 31, 2011

To

my parents,

Ashok and Kalpana Prasai,

for making it possible

to follow my dreams.

ACKNOWLEDGEMENTS

First and foremost, I would like to thank my advisor, Professor Deepak M. Divan, whose support and guidance has made all this work possible. Working with him on the many different projects the last several years has been a great honor and a privilege of mine, as I have learned a great deal both technically and non-technically. He has my gratitude for imbibing in me the skills to identify the right questions to ask, as I have come to know that the right question is always much more difficult to obtain than the right solution.

I would like to acknowledge the rest of my committee members, comprising of Professor Ronald G. Harley, Professor Thomas G. Habetler, Professor David G. Taylor, and Professor J. Rhett Mayor. I have come to see Professors Harley and Habetler as the steady rocks of the Electrical Energy group, sagely guiding and supporting students from the start to the very end of their graduate study. From Professor Harley, I learned all about designing and operating neural networks, swarm intelligence, fuzzy system, and evolutionary computing. I have also had the great pleasure of working with him in a few projects, in which his guidance has proven to be invaluable. From Professor Habetler, I learned about the state-of-the-art approaches to modeling and controlling electrical machines of all forms and types. I am also very thankful to both Professors Taylor and Mayor for their time in evaluating my thesis and providing valuable feedback.

While there are many faculty and staff members who have enriched my graduate experience at Georgia Tech, a few stand out. I am grateful to Frank Lambert for all his guidance he provided in a couple of the projects I worked on with him. Many thanks goes out to James Steinberg for his help in fabricating the various converters

and prototypes I built while I was at Georgia Tech. James has been a valuable asset to our group and a good friend to me, without whom not many of my projects would ever have been successful. I am also thankful to Deborah King for all her help in tackling the logistics of being a graduate student, whether ordering parts and supplies for us to keep our projects running smoothly or ensuring we have room and board for a conference.

I have perhaps learned the most from my fellow students and colleagues. For this, I am grateful to Jyoti Sastry, Harjeet Johal, Yi Yang, Yi Du, Andrew Paquette, Frank Kreikebaum, Rajendra Prasad Kundula, Rohit Moghe, Jorge Herndandez, and Debrup Das. It was only with their help that I had a smooth ride through my doctoral program.

I am especially grateful to Jyoti Sastry for her help and support through the tough times when nothing worked as expected, in life or with my projects. It was only through her patience and encouragement that I was able to overcome each difficulties and rise above to tackle the next.

I am extremely lucky to have parents who have given me their unreserved love and support in all my endeavors throughout my life. They instilled in me many positive qualities that have shaped the man I have become today. I am eternally thankful to them for providing me with the great many opportunities that have led me to this point in my life. To them, I dedicate this thesis, as this work is as much a product of their labor as it is mine. I am also thankful to my sister for cheering me on from the sidelines and for keeping things real for me.

I would like to acknowledge that this work was funded by the Intelligent Power Infrastructure Consortium (IPIC) at Georgia Tech. This work made use of software titles that include Synopsys Saber and MathWorks Matlab, and DSP controller board donated in kind by Texas Instruments.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Reactive power is critical to reliable operation of the modern AC power system. There is a plethora of motor-loads, transformers, and power-electronic loads connected to the power grid, which consume reactive power for normal operation. Transmission lines also consume reactive power when they are loaded above their surge impedance loading (SIL). Reactive power can exact opportunity cost due to reduced capacity of the lines to carry real power, which in turn lowers revenue. Most transmission owners (TOs) levy large penalties against load serving entities (LSEs), industrial facilities, and other end-use customers, who consume more than their allotted amount, as measured by their power factor. These penalties are to incentivize their customers to meet their reactive power needs locally as well as to recuperate the TOs' financial losses.

Harmonic pollution is another factor that prevents the optimal operation of the grid and the connected loads. Harmonics are attributable to proliferation of the diode-rectifier- or thyristor-rectifier-interfaced loads such as variable speed ac drives and power supplies in server farms, electric arc furnaces, and other non-linear loads, which are widely employed by the industrial sector. With wider adoption of harmonic-rich loads by the consumer sector as well, such as HDTVs and compact fluorescent lamps (CFLs), greater level of triplen harmonics associated with single-phase loads are also increasingly seen on the distribution grid. The increasing penetration of renewable resources and electrification of light-duty vehicles are expected to further aggravate the stresses and congestion on the utility grid.

Reactive power compensation is necessary for supporting the AC grid and maintaining a healthy voltage stability margin. Compensation can also enhance the utilization of system capacity, lower system losses, provide fault ride-through, and enable a quick fault recovery. Existing VAR and harmonic compensation technologies are either too expensive or inadequate to meet the dynamic needs of the modern and the future power system.

This dissertation presents a novel class of Dynamic VAR and Harmonic Compensators (DVHCs) for supplying or absorbing reactive power and providing harmonic filtering, where the compensation is in shunt with the line and the load. The underlying concept is based on augmenting a static or passive component like a capacitor or an inductor with a direct AC converter and imbuing the passive component with dynamic properties. The direct AC converter can be configured as a buck, a boost, or a buck-boost. A 'fail-normal' switch is an integral part of the DVHCs that bypasses the converter when it fails, preserving the original functionality and the reliability of the passive component. The DVHCs are modular and scalable such that they can be employed in applications ranging from residential and industrial with voltages less than 480 V, to power distribution level with voltages as high as 35 kV. The Dynamic Inductor (D-IND) and the Dynamic Capacitor (D-CAP) are subclasses of the DVHCs. As the applications for supplying leading VARs are more prevalent, the primary focus of this work is on the buck, the boost, and the buck-boost configurations of the D-CAP.

To understand the characteristics and operation of the DVHCs, this work has developed time-domain models for analyzing the transient and dynamic behavior; frequency-domain models for understanding the harmonic interactions and the steady-state relationships between switch duty and current harmonics; and small-signal models for studying the dynamics of the converter due to various perturbations. The small-signal models also enable extraction of transfer functions in designing controllers

and assessing stability margins.

Control architectures and techniques are presented for effectively controlling the D-CAP when commutating the semiconductor devices with both high and low switching frequencies.

In modularly scaling the DVHCs to higher voltages, three medium-voltage topologies are discussed. They are based on series-connecting fractionally-rated devices, AC flying capacitors, and series cascading multiple two-level cells. These implementations allow direct connect to the medium-voltage grid, thereby obviating the use of transformers, and subsequently reducing the losses, cost, complexity, and footprint. A novel AC snubber concept is proposed to provide safe commutation of the AC switches, fault tolerance by managing the energy trapped in parasitics and filters, and to enable dynamic and static voltage sharing when integrated around the series-connected devices.

Design equations for selecting and rating the devices and components in the buck, the boost, and the buck-boost configurations of the D-CAP are presented. Three sets of example designs, with one at low-voltage and two at medium-voltage, are discussed to demonstrate the typical size and ratings of the various components under realistic operating conditions.

Measurements and the related discussions of a 40 kVA buck D-CAP prototype built to validate the effectiveness of the proposed concepts are presented.

CHAPTER I

INTRODUCTION

1.1 Problem Statement

Reactive power, measured in volt-ampere reactive or VAR, is critical to reliable operation of the modern AC power system. There is a plethora of motor-loads, transformers, and power-electronic loads connected to the power grid that consume reactive power for normal operation. While there is no monetary value associated with providing reactive power to end customers as there is with real power, reactive power can exact opportunity cost from the transmission owners. This is because reactive power lowers the available transfer capacity of the lines to carry real power and in turn lowers the revenue. Most transmission owners (TOs) levy large penalties against load serving entities (LSEs), industrial facilities, and other end-use customers who consume more than their allotted amount, as measured by their power factor. These penalties are to incentivize their customers to meet their reactive power needs locally as well as to recuperate the TOs' financial losses.

Due to the inductive nature of the transmission lines, the grid voltages start to droop when they are heavily loaded. If the voltage falls below a certain threshold, equipment and loads start sustaining damage. If it falls lower, it can induce a sudden system collapse as the grid falls out of stability. Reactive power compensation is necessary for supporting the grid voltage and maintaining a healthy voltage stability margin during both steady-state and fault contingencies. Further, VAR compensation can enhance the utilization of system capacity, reduce system losses, provide fault ride-through, and provide a quick fault recovery.

The issue of harmonic pollution is more complex. While IEEE 519, first formulated

in 1982, specifies the maximum harmonics that can be injected at the point of common coupling (PCC) of industrial facilities, there has been no movement to enforce it unless the harmonics interfere with the neighboring loads. This is primarily because the cost of compliance with existing technologies has been fairly high with no financially-quantifiable benefit for the customer.

On the consumer side over the last decade, the increase in energy consumption has gone hand-in-hand with the increase in size or quantity of non-linear loads such as high definition televisions (HDTVs), computers, compact fluorescent lamps (CFLs), energy-saving appliances such as washing machines, and other harmonic-rich loads. The high demand for these low-cost, high-tech appliances have significantly increased the level of harmonics injected into the grid [90, 56]. While individual homes may not be much of an issue, the aggregated effect of many communities, in combination with the industrial plants that are non-compliant with IEEE 519, is increasingly felt on the distribution level with increases in harmonic levels that trigger false tripping of relays, lower system efficiency, and shorten the life of equipment [40, 68].

The increasing penetration of renewable resources and electrification of light-duty vehicles are expected to further aggravate the stresses on the utility grid. The conventional approach to support the grid-integration of these new sources and loads is to add new base capacity and to build new transmission lines. However, this will only increase the financial burden on the end-use customers, resulting in disillusionment with these 'green' initiatives. Supporting these societal trends requires strategic and incremental deployment of grid-control technologies that have the capabilities to support the dynamic nature of the existing, and emerging sources and loads.

The reactive power technologies on the grid can be divided into two categories: static and dynamic. The static shunt compensators such as capacitors and reactors are installed as part of the transmission and distribution planning. The static solutions, as the term implies, are fixed assets that supply the base reactive power

requirements of the system. These solutions are unable to compensate for the increasing dynamic nature of the power grid with rapid changes in power flow brought on by the new sources and loads. Their capabilities are also very limited during fault contingencies when the grid voltage starts to droop and their reactive power output drops as a square of the grid voltage. For harmonic filtering applications, the static or passive solutions can be quite effective in correcting power factor of loads with a large harmonic signature, but they can be easily overloaded from unintentional sinking of harmonics from the grid or neighboring loads. The existing dynamic solutions such as a static VAR compensator (SVC) and a static synchronous compensator (STATCOM) for providing shunt VAR compensation, and inverter-based active filters for suppressing harmonics have been commercially available for well over two decades. While the SVCs have enjoyed relatively wider deployments, the inverter-based solutions have had a very limited market penetration due to their high cost, despite their higher functionality and better performance.

Unfortunately, the lower costing SVCs are not adequate in addressing the dynamics of the intermittent renewable sources and peaking loads, whose integration are expected to significantly increase over the next couple decades. This is due to SVCs' slow response and a similar curtailment of their maximum output under sub-nominal grid voltages as experienced by the static capacitors and reactors. Furthermore, the SVCs are only cost-effective at high power, have a large footprint, and are generally noisy due to injection of low-frequency harmonics, thereby severely limiting their potential for incremental and distributed deployment at spatially-constrained locations where supply of reactive power are most needed.

What is required is a technology with performance and functionality at par with the inverter-based STATCOMs, but at the cost of the SVCs to meet the emerging challenges of the future grid. The ideal technology would demonstrate high efficiency and high reliability to keep the operation and maintenance costs down as well as

reduce the number of service interruptions. In addition, the technology would have a rugged design to operate under realistic grid conditions in an outside environment with a wide temperature range. The technology would be modular and scalable so it could be deployed incrementally without high design-cost penalties. This is a challenging list of requirements that existing technologies have been unable to meet.

1.2 Research Scope and Objectives

This dissertation presents a novel class of Dynamic VAR and Harmonic Compensators (DVHCs) for supplying or absorbing reactive power and providing harmonic filtering, where the compensation is in shunt with the line and the load. The underlying concept is based on augmenting a static or passive component like a capacitor or an inductor with a direct AC converter and imbuing the passive component with dynamic properties. The direct AC converter can be configured as a buck, a boost, or a buck-boost. A 'fail-normal' switch is an integral part of the DVHCs that bypasses the converter when it fails, preserving the original functionality and the reliability of the passive component. The DVHCs are modular and scalable such that they can be employed in applications ranging from residential and industrial, with voltages less than 480 V, to power distribution level, with voltages as high as 35 kV.

The Dynamic Inductor (D-IND) and the Dynamic Capacitor (D-CAP) are subclasses of the DVHCs. The concept of the Dynamic Resistor (D-RES) is also introduced where a resistor is used for harmonic filtering - a very innovative concept, but lacking an ability to supply or consume reactive power at the fundamental frequency, the D-RES is not considered in a great detail in this work. As the applications for leading VARs are more prevalent, the primary focus of this work is on the buck, the boost, and the buck-boost configurations of the D-CAP. However, both the qualitative and quantitative discussions can easily be extended to the D-RES and the D-IND.

The primary objectives of this research are:

1. To develop time-domain models to understand the transient behavior of the D-CAP.

2. To develop small-signal models to understand the converter dynamics, to design controllers, and to assess the stability margins.

3. To develop steady-state frequency-domain models to understand the harmonic interactions between the control handles and the controlled variables in the active filter applications.

4. To develop a strategy for closed-loop control of the DVHCs to provide VAR and harmonic compensation, and single- and three-phase control architectures to realize it under high-switching-frequency operation.

5. To apply a previously developed strategy for optimally operating the buck D-CAP when utilizing large power devices with low-switching frequency to the boost and the buck-boost configurations.

6. To develop, design, and implement a novel snubber concept for realizing safe commutation and fault tolerance in the DVHCs, thereby addressing reliability issues that have plagued direct AC and AC-AC converters.

7. To develop, design, and implement approaches to scale the DVHCs to realistic grid voltages, which are beyond the ratings of most off-the-shelf power devices.

8. To design, build, and test a 40 kVA experimental prototype of the buck D-CAP for providing VAR and harmonic compensation.

1.3 Outline of Chapters

Chapter 1: This chapter presented the problem statement that has driven the research work disclosed in this dissertation. This was followed by a summary of the scope and objectives of this research.

Chapter 2: The background for this work is provided, discussing advantages and disadvantages of existing state-of-the-art concepts and products for both the static and the dynamic applications. Reactive power and harmonic compensation markets are briefly discussed, evaluating where the gaps exist for new products to emerge and be successful. Ultimately, for a product to be adopted by the market successfully, it must conform to the operating specifications of the intended market, which in this case includes the utility grid. Specifications that the utility companies have come to expect from their grid assets are discussed.

Chapter 3: The DVHCs are introduced in detail, including the D-RES. Practical circuit implementations of these topologies are provided. Mechanisms for providing VAR injection and harmonic filtering are discussed. The differences between the D-CAP, the D-IND, and the D-RES, as well as the differences in the three configurations of the direct AC converter, in providing VAR compensation and/or harmonic filtering are delineated.

Chapter 4: The governing equations of the D-CAP are formulated, and time-domain analytical and numerical solutions are derived.

Chapter 6: The steady-state frequency-domain models of the D-CAP are presented that are able to accurately describe the impact of small variations in the duty-cycle function on the harmonics of the various currents and voltages. As the current delivering reactive power to the grid is of interest, relationships between the harmonic coefficients in that current and the harmonic coefficients in the duty function are established. Through an iterative numerical algorithm, an approach to inversely calculate the duty coefficients for a given set of harmonic coefficients in the current is presented.

Chapter 5: The derivations of the average and small-signal models of the D-CAP are presented. Based on the small-signal models, transfer functions to study converter dynamics are extracted.

Chapter 7: A sensitivity analysis is presented to establish a strategy for controlling the D-CAP. Based on the results of the analysis, single- and three-phase control architectures are presented. The approach to tuning the controllers is described. Based on the transfer functions obtained in the previous chapter, and the controller designed in this chapter, a methodology to assess the stability of the D-CAP under purely VAR compensation applications is presented.

Chapter 8: The concept of selective harmonic cultivation is described where the sinusoidal grid voltages are chopped at precisely calculated angles to inject current in the grid with a specific set of harmonics for providing VAR and harmonic compensation. This approach is extremely powerful when designing DVHCs with large devices that operate with low-switching frequencies.

Chapter 9: Three transformer-less approaches to scale the D-CAP to medium voltages with fractionally rated devices are presented. Their advantages and disadvantages are discussed and their operations are validated through simulation results. A novel concept of an AC snubber is presented for use with bi-directional or AC switches to ensure safe commutation, fault tolerance, and equal voltage sharing with multiple series-connected devices. Two practical implementations of the snubber concept are presented.

Chapter 10: Design equations for sizing and rating the various components and devices in the D-CAP, including the three implementations of the AC snubber, are presented. Based on these equations, three example designs are presented; one for a low-voltage application, and two for medium-voltage applications.

Chapter 12: Concluding remarks summarizing the contributions and knowledge acquired from this research work are presented.

CHAPTER II

BACKGROUND AND PREVIOUS WORK

2.1 Introduction

Reactive power compensators come in two varieties: static and dynamic. The static compensators are provided by fixed capacitors and reactors that are installed on the system as part of transmission planning and whose costs have historically been recuperated through a utility's cost-of-service rates.

The dynamic compensators are provided by technologies such as a synchronous generator and condenser, and flexible AC transmission system (FACTS) such as a static VAR compensator (SVC) and a voltage-source-inverter-(VSI)-based static synchronous compensator (STATCOM). The term "static" in the latter two FACTS technologies are used to denote technologies with solid-state switches as opposed to ones built with rotating machines as in the case of synchronous condensers. This work instead uses the term static to mean the opposite of dynamic.

The dynamic solutions are critical for ensuring milliseconds-to-minute stability of the system because load and diversity profiles and in turn the reactive power requirements can fluctuate rapidly, and sometimes unexpectedly, throughout the day. Dynamic supply of reactive power becomes even more critical during fault contingencies when a large amount of fault current can rapidly degrade the voltage stability margin within a few cycles. An adequate supply of reactive power can support the grid during a contingency while the protection and control system identifies and isolates the fault. Dynamic compensation will also be important in supporting grid operations with increased penetration of renewable resources such as wind and solar photovoltaic systems, which are driven by the renewable portfolio standards (RPS)

and electrification of the transportation sector. These new intermittent sources and peaking loads are expected to significantly stress the stability and efficiency of the system.

Although capacitors and reactors are at least a whole order less expensive than the dynamic compensators, their functionalities are also very limited. They cannot respond to dynamic reactive power requirements of the system, and in contingencies, will provide even less reactive power due to the supply dropping as a square of the decreasing grid voltage. The dynamic compensators are much more expensive to own and operate but can react rapidly to emerging contingencies and power flow changes. However, both the SVCs and the STATCOMs only scale in cost at high power levels, and thus are not cost effective at lower power levels where they could be deployed incrementally in a distributed fashion. The mechanically-switched capacitors (MSCs) and the thyristor-switched capacitors (TSCs) are therefore more prevalent at the lower voltage and power levels. Similar to capacitors, the maximum reactive power injection drops as a square of the voltage for the MSCs, the TSCs, and the SVCs, which poses a serious limitation during fault contingencies when compensation is most required. The STATCOMs are more costly than the SVCs, but they have a smaller footprint and can maintain one per-unit of reactive current even when the grid voltage starts to sag. They can also provide power flow control and oscillation damping in certain configurations.

Although the technical viability of STATCOMs and the other inverter-based compensators has been validated through many demonstration projects, their market penetration has been abysmal. Most utility companies have preferred the SVCs, despite their inferior performance, due to their lower costs. They have found it difficult to justify the cost versus the added functionality of the STATCOMs.

Similar to the reactive power compensation technologies, there are static (passive)

and dynamic (active) solutions for harmonic filtering as well. The passive technologies consist of single-tuned and high-pass filters that provide low impedance path for the harmonics in the load, thereby preventing the harmonics from corrupting the grid voltages at the PCC and interacting with sensitive loads. The active filter market is entirely dominated by the inverter-based solutions, which provide filtering by synthesizing currents in anti-phase with the load harmonics. While the passive solutions are less costly than the active and are as effective in filtering harmonics, they can easily be overloaded by sinking unintended harmonics from the grid. Hybrid solutions attempt to address this limitation by including a fractionally-rated active circuit whose sole purpose is in preventing the grid dynamics from overloading the passive solution. Nevertheless, both the hybrid and the active filters have historically been deemed too costly for the benefits that they provide.

This chapter examines some of these VAR and harmonic compensation technologies in a little more detail and identifies their strengths and weaknesses. The present reactive power and the harmonic filter markets are also discussed in an effort to identify opportunities to make an impact for a new emerging technology.

2.2 Principles of Compensation

A simple 2-bus model is demonstrated in Figure 2.1 as a one-line diagram where power is being transferred from bus 1 to bus 2. Bus 1 is assumed to be an infinite bus and therefore can source any amount of real and reactive power. Bus 2 is the feeder point for an arbitrary load pocket. The line impedance is modeled with a reactance, X. The phase angle at bus 1 is $\delta_1 = 0$. The real and reactive power received at bus 2 are expressed by,

$$P_2 = 3V_1V_2b\sin(\delta_2), \tag{2.1}$$

$$Q_2 = 3bV_2^2 + 3V_1V_2b\cos(\delta_2), \tag{2.2}$$

where

$$V_1 \equiv \text{magnitude of line-to-neutral voltage at bus 1,}$$

$$V_2 \equiv \text{magnitude of line-to-neutral voltage at bus 2,}$$

$$\delta_2 \equiv \text{phase angle at bus 2,}$$

$$b = -\frac{1}{X}.$$

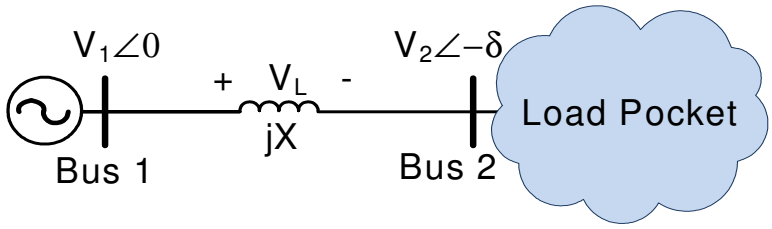


Figure 2.1: One-line diagram of two buses connected by a single line.

The voltage magnitude at the receiving bus is then given by,

$$V_2 = \sqrt{\frac{6\alpha b P_2 + 9b^2 V_1^2 \pm \sqrt{\left(6\alpha b P_2 + 9b^2 V_1^2\right)^2 - 36b^2\left(1+\alpha^2\right)P_2^2}}{18b^2}}, \tag{2.3}$$

where α is a ratio of reactive power over real power drawn by the load pocket, or $\alpha = Q_2/P_2$. The reactive power sourced by bus 1 to support the power transfer, P_2 and Q_2, is calculated as:

$$Q_1 = \Im\Big(-3\mathrm{j}b\tilde{V}_1\left(\tilde{V}_1^* - \tilde{V}_2^*\right)\Big), \tag{2.4}$$

where

$$\tilde{V}_1 = V_1 e^{\mathrm{j}\delta_1},$$

$$\tilde{V}_2 = V_2 e^{\mathrm{j}\delta_2}.$$

The maximum power transfer capability of a line occurs when $\delta = \pi/2$ and is expressed as:

$$P_{max} = \frac{3b}{2}V_1^2\left(\alpha - \sqrt{1+\alpha^2}\right). \tag{2.5}$$

Real power transfer capability over a line is demonstrated using an example case scenario. For the voltage magnitude at bus 1 of $V_1 = 115/\sqrt{3}$ kV and the line impedance of $X = 33.06\Omega$, the reactive power sourced at bus 1 and the voltage magnitude at bus 2 versus the real power transferred from bus 1 to bus 2, which is varied from 0 to P_{max}, are listed in Table 2.1. The load pocket connected to bus 2 is assumed to have unity power factor such that $\alpha = 0$.

Table 2.1: Voltage and reactive power received at bus 2 versus real power transferred from bus 1 at 115 kV with the line reactance of X = 33.06 Ω.

Power Transferred (MW)	Voltage at Bus 2 (kV)	Reactive Power From Bus 1 (MVAR)
0	66.40	0
40	66.06	4.041
80	64.99	16.69
120	62.99	40.00
160	59.39	80.00
200	46.95	200

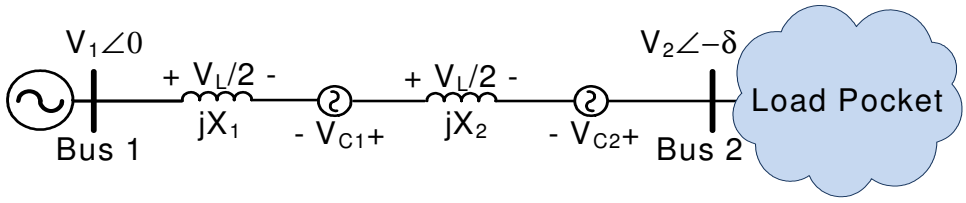
A few notable characteristics are observed in this example:

- The maximum power transfer capability is limited by the line impedance and peaks at $\delta = \pi/2$.
- As more power is pushed through the line, the more reactive power is consumed, until the real and reactive power transferred equal each other at $\delta = \pi/2$. However, lines typically hit their thermal capacity much sooner because of the I^2R losses that limit the maximum current on the line and subsequently the maximum power.
- The voltage at the receiving bus starts to droop significantly with the increasing amount of reactive power consumed by the line. Sub-nominal voltages can damage equipment and cause higher losses as constant power loads attempt to draw more current due to the lowered voltage. As the loading increases and the

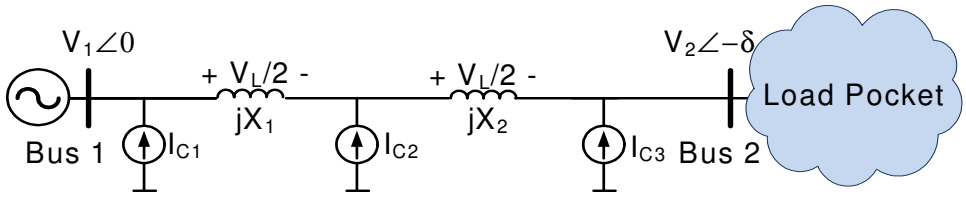
voltage droops further, a cascading effect can occur where the loads continue to draw even higher amount of current, aggravating the droop and eventually leading to a voltage collapse.

To support the voltage at the receiving bus and ensure adequate voltage stability margin exists, the reactive power compensation is applied in either series or shunt. The series compensation, depicted in Figure 2.2(a), effectively injects a voltage in series with the line to cancel out the drop across the line impedance and subsequently maintain voltage at bus 2 within a nominal band. In other words, the series compensation tries to minimize the effective reactance of the line, thereby increasing the maximum power transfer capacity, and reducing the voltage drop across it.

The shunt compensation, exemplified in Figure 2.2(b), injects current in parallel or shunt with the source and the load. The current can either be leading or lagging, depending on the type of compensation required. For the previous example, a leading (or capacitive) current is injected to supply the reactive power consumed by the line. The solution can be distributed as in the figure, or it can be installed at a particular location to supply downstream.



(a) Series compensation



(b) Shunt compensation

Figure 2.2: Reactive power compensation through series and shunt configurations.

If the load pocket also consumes reactive power, without compensation, that power

has to be delivered from bus 1. Due to the inductive nature of the line, only so much reactive power can be supplied from bus 1 before the line reaches its thermal limit. Generators are also limited by their rated capacity. Because there are no charges to customers for supplying reactive power, the generator accumulates opportunity cost, or loss of revenue from not being able to sell real power. Therefore, transmission owners require loads to maintain their power factor close to unity by meeting their reactive power needs locally. In Figure 2.2(b), the current, I_{C3}, from the third compensator can supply reactive power locally to the load pocket, without having it delivered through the line and causing voltage drops, line losses, and reduction in the real power transferred.

Harmonic pollution is the second issue that prevents the optimal operation of the grid and the connected loads. Harmonics are attributable to proliferation of the diode-rectifier- or thyristor-rectifier-interfaced loads such as variable speed AC drives and power supplies in server farms, electric arc furnaces, and other non-linear loads, which are widely employed by the industrial sector. With wider adoption of harmonic-rich loads, such as HDTVs and CFLs by the consumer sector, a greater level of triplen harmonics associated with single-phase loads is also increasingly seen as a problem on the distribution grid.

Total harmonic distortion (THD) measurements on a line current made over a period of 12 months in a 15-min interval on a 12 kV line within a substation located in Alabama are shown in Figure 2.3. The plot reveals THD varying anywhere from about 10 to 50 percent over a year. While the harmonics were quite significant at this particular substation, a Southern Company engineer believes that THD of 3 to 10 percent observed at several other locations in Alabama are quite representative of the harmonics on the distribution grids which are believed to be increasing rapidly year-to-year [75].

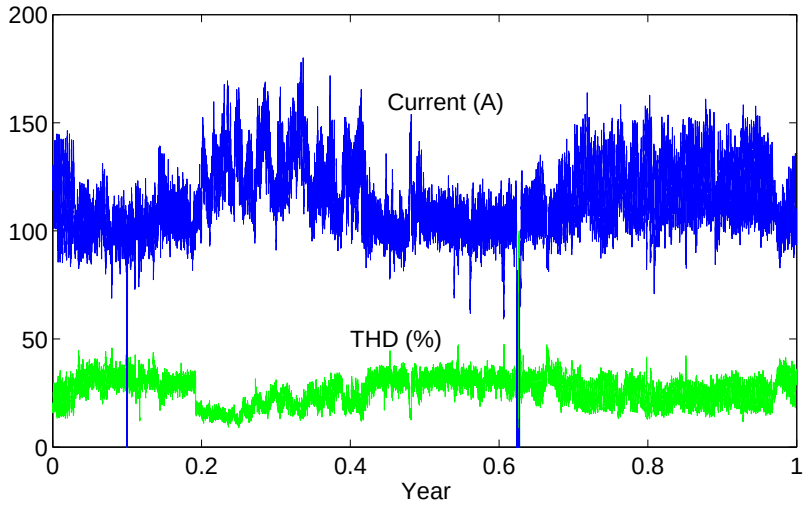


Figure 2.3: Line current and its THD measurements on a 12 kV feeder within a substation located in Alabama, where measurements are made on a 15-min interval spanning from September 15, 2010 to September 15, 2011.

Similar to the supply of reactive power at the fundamental frequency, the harmonics can be compensated in either series or shunt. The series compensation is targeted more for decoupling the grid and its harmonic from interacting with the loads, where voltages that are in anti-phase with the harmonic voltages on the grid are synthesized such that only a clean sinusoidal at the fundamental frequency is seen by the loads. The shunt compensation targets the harmonic producing loads directly by locally addressing the reactive power requirements of the load at specific odd harmonic frequencies.

The series compensation is ideally suitable for when the system is first being built. If the compensation is introduced later, it requires de-energizing of the lines as the device is added in series. A thorough survey of the system is required when employing passive compensators such as the capacitors, as an inappropriately selected component can induce sub-harmonic resonances. The active solutions can prevent unwanted resonances and can provide additional features such as power-flow control and oscillation damping. However, active solutions such as the unified power-flow

controllers (UPFCs), the static synchronous series compensators (SSSCs), and the interline power-flow controllers (IPFCs) utilize series transformers. Under fault conditions, when a large amount of current is flowing through and saturating the transformer, functionality is lost during a period when compensation is most required.

Due to these drawbacks with the series compensation, this work will focus exclusively upon the shunt solutions. The next several sections will examine some of the more popular technologies for providing VAR and harmonic compensation.

2.3 Technologies for VAR Compensation

2.3.1 Static Solutions

The static assets for injecting reactive power into the grid are the lowest-cost solutions due to their simplicity. These assets are often installed ubiquitously and are an integral part of transmission and distribution planning. They are generally factored into the cost of building new lines and recuperated through the utility's rate base.

Capacitors provide the most common form of reactive power compensation to offset the inductive nature of the power grid and supply reactive power to the inductive loads, thereby improving power factor, voltage stability, available transfer capacity, and reducing network losses. Lagging VARs, in the form of reactors (inductors), are often required for compensating the capacitive charging of the high voltage and lightly loaded lines, and ensuring that the line voltages do not rise above the accepted levels. Both the static capacitors and the reactors are typically connected directly to the line. Direct-connect designs are generally less costly because the complexity and footprint of the products are minimal. The lack of moving or switching elements is also a contributing factor to their low cost and robust designs.

2.3.1.1 Shunt VAR Capacitors

The shunt VAR capacitors, such as the ones shown in Figure 2.4, are installed at strategic locations where reactive power compensation are typically required. The injected three-phase reactive power depends on the voltage imposed across the capacitor as given by,

$$Q = V_{LL}^2 \omega C,$$

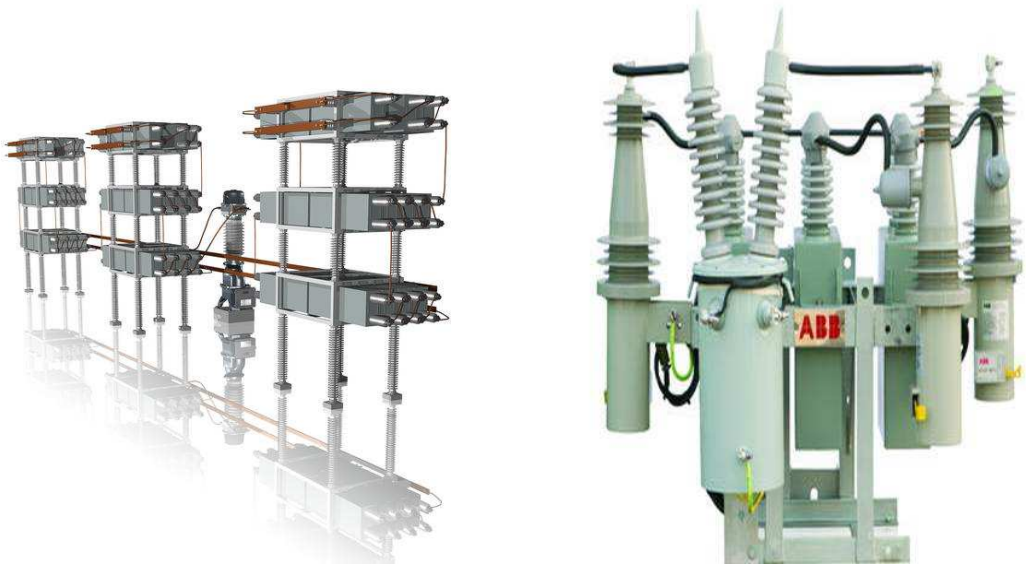
where

$Q \equiv$ leading VARs injected,

$V_{LL} \equiv$ line-to-line grid voltage,

$\omega \equiv$ line frequency in rad/s,

$C \equiv$ value of the equivalent capacitor connected line-to-neutral.



(a) Open-rack shunt-VAR capacitors (b) Pole-mounted capacitors

Figure 2.4: ABB's three-phase shunt-VAR capacitors (photo courtesy of ABB).

During fault contingencies, when the grid voltage sags and a greater supply of reactive power is required to support the grid, the output drops as a square of the

voltage. Further, capacitors are unable to track the reactive power requirements of the constantly fluctuating loads connected to the grid, thereby injecting more power than necessary at certain times, and not enough during other times.

The sizing of the capacitors requires an engineering survey of the electrical environment in which they will be installed. An inappropriately selected value could lead to source-sink resonances induced by the disturbances on the grid such as load steps or faults. The static capacitors can also worsen the harmonic signature of the line current by injecting harmonic current at the same frequencies as the harmonic contents of the grid voltage,

$$I\left(n\omega t\right) = V\left(n\omega t\right) n\omega C e^{j\pi/2}.$$

The cost of the shunt VAR capacitors today are typically around $10 to 20 per kVAR [43, 81, 58].

2.3.1.2 Shunt Reactors

A static shunt reactor, similar to the one shown in Figure 2.5, are installed to compensate for the capacitive nature of the high-voltage and lightly-loaded lines. The shunt reactors share some of the same set of advantages and disadvantages as the shunt VAR capacitors. Their simplicity leads to robustness, high reliability, and low costs. However, their static nature limits them from varying the level of compensation to match the dynamic nature of the power system and in turn regulate the system voltages. For this reason, these reactors are also equipped with mechanical switches that allow them to be brought in and out at very slow rates to provide reactive power balance on the system.

The typical cost of the shunt reactors are in the range of $20 to 30 per kVAR [43].

Figure 2.5: A shunt reactor brand-named by Siemens (photo courtesy of Siemens).

2.3.2 Dynamic Solutions

Dynamic assets that can be varied within a few cycles are required in applications where the static solutions are inadequate in meeting the system's dynamic needs. These applications in the past have predominately existed at the interfaces of industrial facilities with rapidly changing load levels and power factors. However, with increasing mandates and regulations requiring a greater level of renewable integration, dynamic assets will be increasingly needed at the transmission and distribution level to cost-effectively compensate for the expected increase in the spatial and the temporal variability of the non-dispatchable renewable resources. As of August 2011, 28 states have adopted the Renewable Portfolio Standards (RPS) requiring anywhere from 10 to 33 percent of their electricity generated to come from renewable sources by 2030 at the latest [83]. The more costly alternative to support the grid integration of renewables is to install additional dispatchable generation and transmission capacity. Even if costs were not a factor, obtaining the right-of-way and allocating adequate capital to build new lines and generators can be a lengthy process. While

some amount of new transmission and generation build-outs are inevitably required, their numbers can be reduced through strategic deployments of dynamic compensators that are able to alleviate reactive power requirements of the new sources and the loads while strengthening the overall system.

However, the existing dynamic solutions are either too costly, or do not scale well to higher voltages technically and/or economically.

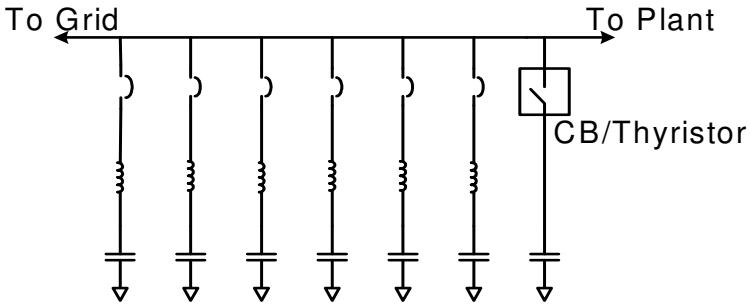
2.3.2.1 Switched Shunt VAR Capacitors

Industrial plants often use the switched shunt-VAR capacitors for power factor correction [12, 77, 28, 72, 37]. A single line diagram of a typical industrial installation is shown in Figure 2.6. To realize controllable reactive power and maintain the desired power factor, a bank of 6 to 10 capacitors are incrementally switched in using electromechanical switchgear or contactors. These solutions are called mechanically switched capacitors (MSCs) and are adequate for relatively slow varying loads. In order to avoid source-sink resonances between the capacitors and the line impedance, each capacitor is connected in series with a reactor tuned to the 4.5-th harmonic frequency [54]. Mechanical switching of capacitors can introduce transients with response time often measured in multiple line cycles. Further, the limited mechanical life of contactors are also not suitable in applications with rapidly varying loads.

An alternative is to use the thyristor-switched capacitors (TSCs), where by controlling the turn-on angle of the thyristors, the inrush current and the subsequent transients can be controlled and suppressed. The duty ratings of solid-state switches also make them suitable for compensating rapidly varying loads that require frequent switching. However, even then, the dynamic capabilities of the switched capacitor banks are still very limited as they can only inject reactive power at fixed discrete steps. Further, during periods when greater compensation is required, the maximum injection level drops with a square of the decreasing voltage. While such a solution

may be adequate for most industrial applications, the lack of vernier control and inability to maintain one per-unit reactive current when faced with drooping grid voltages can impact the voltage profile and stability margin of the grid, subsequently leading to sub-optimal system operations, higher system losses, and danger of system collapse lacking adequate compensation. This approach also does not scale well without a step-up transformer to higher voltage applications where a direct connection to the medium-voltage lines is desirable.

(a) Picture of a switched capacitor bank



(b) Schematic of a switched capacitor bank

Figure 2.6: Switched capacitor banks employed for power factor correction by industrial plants.

The typical cost of TSCs are in the range of $30 to 50 per kVAR [43, 81, 58].

2.3.2.2 Synchronous Condensers

The synchronous condensers are one of the oldest technologies for providing dynamic VAR compensation. The technology is a synchronous motor that through the control of its field excitation, can be made to either generate or absorb reactive power. The inherent inertia of the machine can act as a shock absorber to the disturbances on the grid. The typical installation cost is in the range of $10 to 40 per kVAR with power rating in the range of 20 to 200 MVAR [43, 26]. Existing synchronous motors and generators in service may be dually employed to provide VAR compensation should they not be fully utilized, thereby alleviating the cost associated with procuring a

machine to exclusively supply reactive power.

However, synchronous condensers have several drawbacks. They are relatively very lossy compared to other dynamic solutions. Typical losses are around 4 to 5 percent of the nominal rating that, in the absence of a good thermal management system, can limit the reactive power capability and the operating duty [86]. Depending on the cost of electricity, these losses also lead to high variable operating costs.

Although the three-phase synchronous machines are able to operate under unbalanced grid conditions, their ability to inject unbalanced compensation is limited. If the voltage unbalances become severe, the machines can also fall out of synchronization. Furthermore, the same inertia that acts as a shock absorber to the disturbances on the grid also limit their response time to vary the supply of reactive power.

In addressing the limitations of the synchronous condensers, the company American Superconductor attempted to commercialize a synchronous condenser technology built using a 1 G high-temperature superconductor (HTSC) called a SuperVAR®. An 8 MVA prototype at 13.8 kV, shown in Figure 2.7, was demonstrated for the Tennessee Valley Authority (TVA) in Gallatin, Tennessee in December 2003 to address the problem of voltage flicker caused by electric arc furnaces. The prototype was capable of providing continuous ±8 MVAR of compensation with up to 6 times the nominal rating for up to 10 line cycles for transient events and up to 2 times the nominal rating for up to 1 minute for low-voltage events. The losses were estimated to be 1.7 percent of the nominal rating, or 136 kW, with an efficiency of 98.3 percent. The whole unit could fit within a 40-ft long trailer [10]. The commercial unit was to be rated at 10 to 12 MVA and initially cost around $100 to 120 per kVAR. There were talks to design a SuperVAR with 2 G HTSC so that the cost could be brought down to $10 to 12 per kVAR, but this never materialized [11]. However, American Superconductor has since then disbanded plans to commercialize SuperVAR entirely.

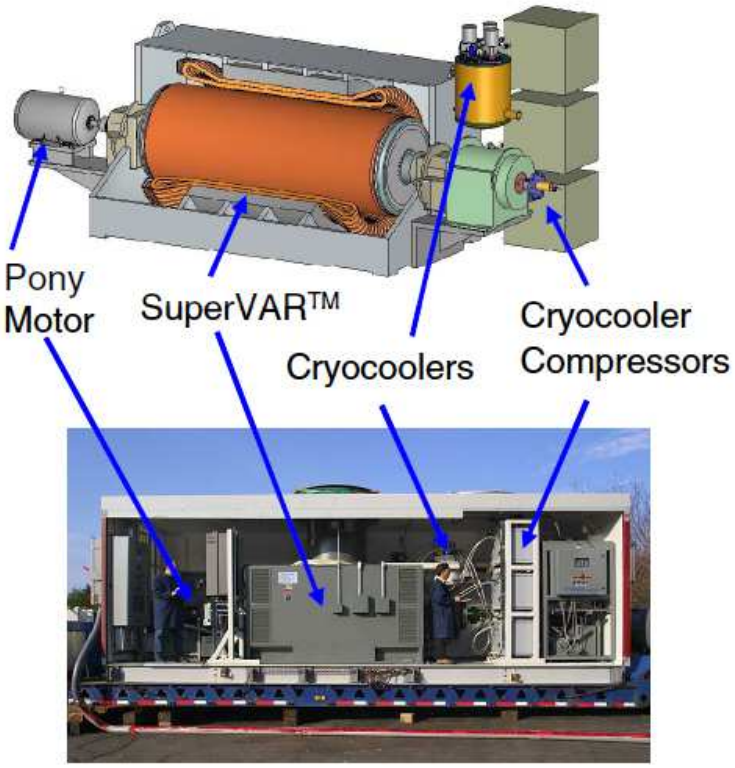
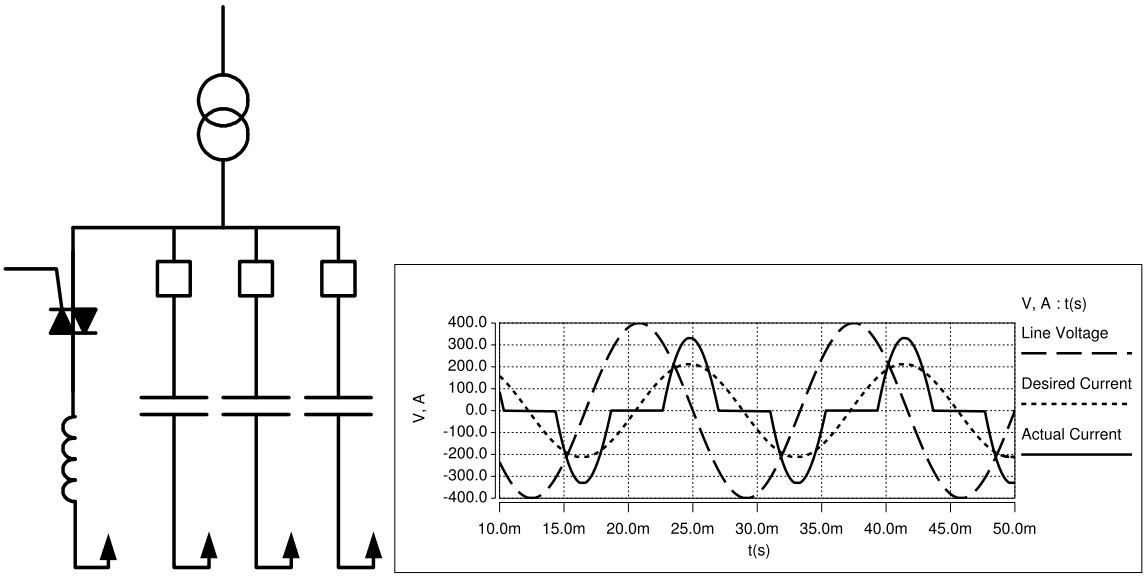


Figure 2.7: American Superconductor's 13.8 kV / 8 MVA SuperVAR prototype system demonstrated at Gallatin, Tennessee for TVA [10].

2.3.2.3 Static Var Compensator (SVC)

The Static VAR Compensator (SVCs) built using the thyristor-switched reactor (TSR) and fixed capacitors has been available for over 30 years and is shown in Figure 8(a) [35, 17, 9, 4, 31]. The unit operates by applying the appropriate number of capacitors for base reactive power injection, and then controlling the firing angles of the TSR to inject lagging VARs, thereby allowing the effective or total reactive power supplied by the unit to be dynamically controlled on a half-cycle to half-cycle basis. The fundamental component of the inductor current injected by a TSR is expressed by Equation (2.6). Lagging VAR compensation is also possible by reducing the number of capacitors that are grid-connected, and if required, by replacing some of these capacitors with reactors.



(a) One-line diagram (b) Current injected by the thyristor-switched reactor

Figure 2.8: Schematic and characteristic waveforms of a Static VAR Compensator (SVC).

$$I_{LF}(\alpha) = \frac{V}{\omega L}\left(1 - \frac{2}{\pi}\alpha - \frac{1}{\pi}\sin(2\alpha)\right) \tag{2.6}$$

The biggest drawback of this concept is that there is a significant amount of harmonics present in the injected current as depicted in Figure 8(b). The harmonic content becomes worse with the increasing firing angle, as given by Equation (2.7), where the maximum amplitudes of the 3rd, the 5th, the 7th, the 9th, the 11th, and the 13th harmonics are 13.78 percent, 5.05 percent, 2.59 percent, 1.57 percent, 1.05 percent, and 0.75 percent, respectively, of the maximum fundamental current magnitude [31]. Therefore, large harmonic filters and transformers are required to not only suppress the harmonics from propagating into the grid, but also to mitigate the resonances and undesired interactions with the line impedance and the capacitors.

$$I_{Ln}(\alpha) = \frac{V}{\omega L}\left(\frac{\sin(\alpha)\cos(n\alpha) - n\cos(\alpha)\sin(n\alpha)}{n(n^2-1)}\right) \tag{2.7}$$

The SVCs also exhibit similar reactive power supply constraints as static capacitors and reactors when the grid voltage starts to droop. This characteristic severely limits the SVC's ability to support the grid during rapid fluctuations of power flow. Therefore, surplus capacity is necessitated in addressing this limitation, subsequently increasing size and cost of the system.

The SVCs are often connected to medium- and high-voltage grids with a step-up transformer, which further increases their cost and footprint. Design and layout of the SVC systems are typically very project specific and highly customized, which further adds to the bottom-line cost. More than thirty SVCs have been installed in the United States with power levels ranging from 30 to 650 MVAR [26]. While the operation and maintenance (O&M) costs are higher than the capacitor banks, they are lower than the generators and the synchronous condensers.

An example installation is shown in Figure 2.9, which is a 525 kV SVC installation by Siemens at the Devers 500 kV substation near Palm Springs, California. The depicted SVC can inject -100 (inductive) to +330 (capacitive) MVAR with two TSRs, three TSCs, and two sets of filters tuned to the 5th and 7th harmonics. Thyristors rated at 8 kV / 4 kA and four step-up transformers rated at 100 MVA each are employed. The low-voltage side of the SVC with the current ratings of 4 kA requires busbars, cables, and transformer and protection equipment wiring with a large cross-section, inflating the cost and the size of the system.

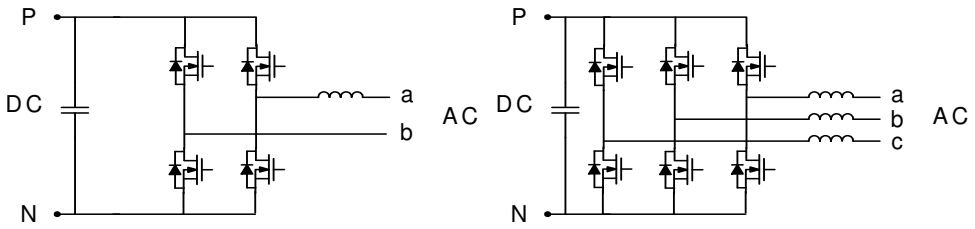
The typical cost of SVCs that allow rapid switching between the reactors and the capacitors are in the range of $40 to 60 per kVAR [43, 81, 58].

2.3.2.4 Static Synchronous Compensators (STATCOMs)

Static synchronous compensators (STATCOMs), based on the voltage source inverters (VSIs), have been commercially available for over a decade [57, 41, 62, 14]. The

Figure 2.9: Siemens SVC installation in the Devers 500 kV substation near Palm Springs, California (photo courtesy of Siemens).

schematics of a single- and three-phase VSIs for low-voltage applications are demonstrated in Figure 2.10, and a three-phase configurations for a high-voltage application is depicted in Figure 2.11. The former figure depicts two-level topologies, while the latter figure shows a 48-pulse converter where each of the four cells are built using a three-level, three-phase VSI. The operating principle behind the STATCOM, and the VSIs in general, is depicted in Figure 2.12, where the difference between the grid and the VSI output voltage imposed across the filter inductor drives the desired current to flow. By controlling the current to either lead or lag the grid voltage by 90 degrees, reactive power can either be supplied or consumed, respectively.



(a) Single phase (b) Three phase

Figure 2.10: The single-phase and three-phase two-level implementations of the voltage source inverter.

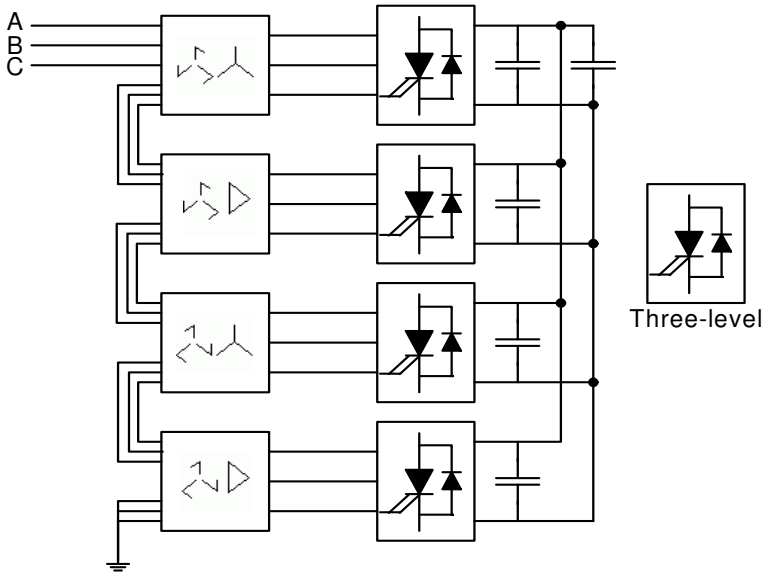


Figure 2.11: Schematic of a STATCOM realized using 48-pulse voltage source converter, where each of the four cells are built using a three-level, three-phase voltage source inverter.

STATCOMs are typically designed for high-power utility applications due to cost-scaling benefits. Therefore, they are considered to be too expensive for use in low-voltage applications. STATCOMs with power ratings ranging from 30 to 100 MVAR have been installed in over seven locations around the United States with the grid-connect voltages of up to 350 kV [26]. A closely related but an even more expensive technology for both shunt and series compensation is the unified power flow controller (UPFC), which has seen two installations in the United States, one at an AEP station and another at a NYPA station.

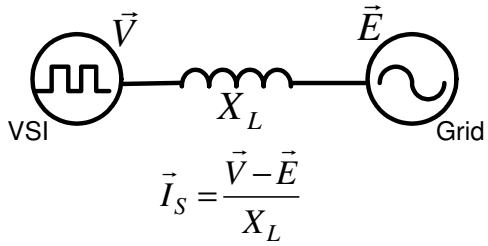


Figure 2.12: The voltage, V, is synthesized based on the desired current, I_S, in a VSI.

While the premium-priced STATCOMs respond more quickly, exhibit a smaller footprint, and have a better THD performance in comparison to the SVCs, their losses are generally higher due to switching of the semiconductor devices.

Their reliability is also poorer due to the very tough requirements on the DC capacitors. The DC bus voltage must maintain a relatively low ripple, typically in the range of 5 to 10 percent, in order to accurately synthesize the reference current or voltage waveforms. This is especially troublesome when there is an imbalance in either the line voltage or the current in the three-phase implementation. The majority of the faults that occur on the system are asymmetrical [66] which lead to the unbalance conditions. A STATCOM is expected to provide a nominal one per-unit of reactive current for all line conditions, especially when the grid is weak and or collapsing due to a fault on the system. Therefore, the energy storage has to be rated large enough to operate even under the worst case imbalances with a low DC voltage ripple. For that reason, DC capacitors with high energy densities are required to ensure that the DC voltage does not deviate by more than 5 to 10 percent over the period of the pulsating DC current. Further, due to the inherent characteristics of the DC side current in the VSI, capacitors that are capable of sourcing and sinking currents with a high dI/dt are required. These various requirements, in combination with the need for a low-cost design, lead to the only obvious bulk energy storage solution: electrolytic capacitors.

While the electrolytic capacitors have become the de-facto standard in inverters due to their low price points, they have also plagued power electronic engineers with their relatively low reliability and high failure rates in grid applications. This is especially significant when compared to standard grid assets that are typically rated to last for 30 to 50 years. A quick glance at their datasheets reveals that these capacitors typically conform to their ratings for 5,000 hours when operated at or below 85 degrees Celsius, compared to 100,000+ hours for polypropylene (film) capacitors used in power factor correction applications. This is because one of the biggest failure mechanisms

is the drying-out of the electrolytic solution in these capacitors due to evaporation from operation above the rated temperature, high levels of inrush current or spikes leading to temperature increase, and aging, etc. [36, 34, 30, 46]. This factor de-rates their energy densities, which can subsequently contribute to sub-nominal inverter performance and cause the inverters to become unstable under certain situations. In alleviating these issues, temperature-controlled environments with heat exchangers are typically required, which contribute to the high cost and the large footprints of the installations. Various papers have been published proposing techniques to minimize the size of the DC capacitor [76, 32, 3]. Other papers have looked at eliminating the use of the inverters entirely and using direct AC-AC converters like the matrix converters that do not require DC storage [42, 44, 50, 60, 29, 61, 87].

For the single-phase implementations, while the issue of imbalances does not exist, the presence of a large, low-frequency, rectified DC current necessitates an even larger DC capacitor to maintain a low-voltage ripple. Companies like AREVA have determined that the benefits versus the cost of a single-phase chain-link STATCOMs, schematically depicted in Figure 2.13, are justified well enough to commercialize them, even with the DC capacitors with energy ratings 10 times more than their three-phase counterparts.

The installed cost of the STATCOMs in large systems rated at over 100 MVAR are typically around $55-70/kVAR [43]. American Superconductor manufactures a modular STATCOM technology under the name Dynamic VAR or D-VAR® that they advertise is superior to conventional STATCOMs due to its improved monitoring, control, response, and ability to deploy incrementally. The modular 8 MVAR D-VAR unit is shown in Figure 2.14, which can be scaled to over 100 MVAR through paralleling. While much of the technology is proprietary in nature, the installed cost is estimated to be around $80 to 100 per kVAR with the price becoming more competitive at higher capacities [43, 26]. Currently, the D-VAR system is targeted

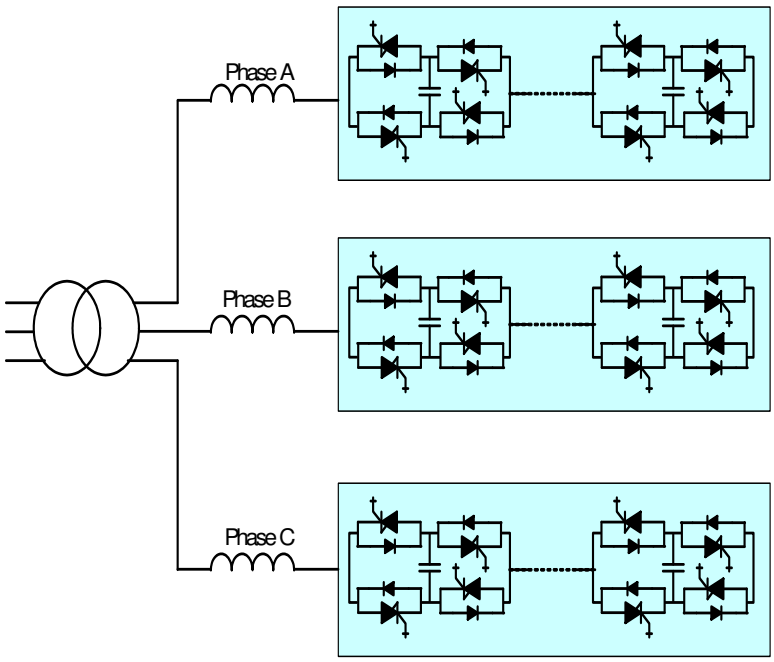


Figure 2.13: Chain-link STATCOM manufactured by AREVA based on a single-phase building-block module.

for the wind industry to strengthen the grid against the intermittent nature of wind energy. These costs do not account for maintenance, repairs or replacement, as will be required with greater frequency when compared to the static assets. There have been over 22 installations of the D-VAR systems in the North America [26].

2.4 Technologies for Harmonic Filtering

The harmonic filtering technologies have traditionally been applied at the vicinity of the harmonic producing loads, such as at load feeder points in industrial and other high power consuming facilities. Loads such as the diode- or thyristor-rectifiers, cyclo-converters, and electric arc furnaces have often been identified as major contributors of harmonics. These loads are generally three-phase with the 5th and the 7th as the primary harmonics.

Single-phase loads also generate harmonics but their contribution in the past have been deemed to be negligible and therefore historically have not been classified as

Figure 2.14: American Superconductor's modular 8 MVAR D-VAR unit (photo courtesy of American Superconductor).

harmonic polluters [2]. However, over the last decade, due to proliferation of low-cost energy-saving appliances on the consumer end, such as CFLs, HDTVs, washing machines, and other non-linear loads, the level of harmonics injected by these single-phase loads have dramatically increased. The aggregated effect of these loads from many communities are increasingly felt on the distribution level with the presence of the third harmonic [40].

The harmonic filtering technologies for suppressing harmonics can generally be categorized into three major technology groups: passive, active, and hybrid active filters. The passive filters continue to be the most widely used solution due to their simplicity, reliability, and low cost. However, the passive filters are very much a custom solution that is extremely site-specific, which can lead to a hefty engineering cost. This is because improperly tuned passive filters can lead to series and/or parallel resonances with the power system and inadvertent sinking of harmonics from the neighboring loads, both of which can overload the filters and render them ineffective.

Active filters attempt to address these limitations by presenting a high impedance

path to the unwanted harmonics/resonances, and a low impedance path for the harmonics of interest. However, the pure active filters are generally more costly than their pure passive counterparts, and aside from low-voltage applications, they have not seen significant deployment at medium voltages [1, 2].

Hybrid active filters combine the desirable salient features of the pure active and passive technologies. This type of a filter consists of a passive filter with a fractionally-rated active circuit in series. The active circuit presents a high impedance to the unwanted harmonics and resonances, thereby preventing the passive filter from overloading.

2.4.1 Static Solutions

Harmonic filtering has historically been achieved using passive filters that are either tuned to a particular frequency or designed as a high-pass filter or a combination of both, where the filters are built using inductors, capacitors, and resistors, as shown in Figure 2.15. This technology has generally been the most cost effective approach to filtering in low-, medium-, and high-voltage applications.

The filters, in the presence of the nearby non-linear load, act as a low-impedance path for the currents at the tuned frequencies. The low impedance is affected by the quality factor, Q, of the filter, which for the single-tuned filters range from 20 to 100 [51]. In a typical installation, four single-tuned filters target the 5th, the 7th, the 11th, and the 13th harmonics while a second-order high-pass filter is tuned to suppress the 17th and the higher order harmonics. Although the high-pass filter provides better filtering performance over a wide range of frequencies, it is also generally lossier at the fundamental frequency than the single-tuned filters.

The passive filters are severely limited in their performance due to several factors. These factors include temperature variation of the component values, manufacturing tolerances that, at best, are typically plus/minus 5 percent, and unwanted resonances

with the grid impedance and inadvertent sinking of currents from the grid or other nearby non-linear loads that attempt to overload the filters and de-rate their capability or, worse, render them completely ineffective. For that reason, the site has to be extensively surveyed before an installation.

To alleviate the cost of providing filtering or VAR compensation alone, the filtering and power factor correction functionalities are usually packaged together as a single product.

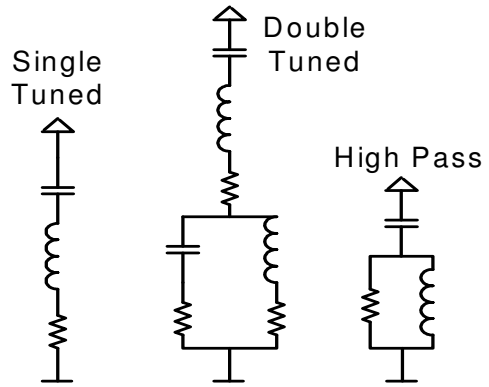


Figure 2.15: Tuned and high-pass passive filter topologies.

2.4.2 Dynamic Solutions

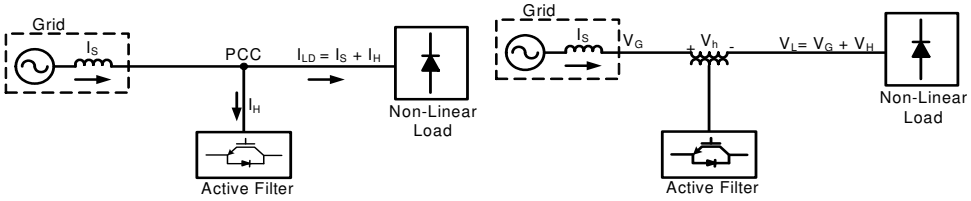
2.4.2.1 Pure Active Filters

To address the limitations of the passive filters, active filters designed using VSIs have been studied extensively since the 1970's. These filters provide dynamic, robust, and versatile performance at a smaller footprint [1, 8, 23, 13]. Filters built using the current source inverters (CSI) have also been studied, but their cost, size, and losses are larger compared to the VSIs, which have limited their applications.

Although the active harmonic filtering technologies have been available in the market for over 20 years, market penetration has been very limited due to poor reliability and high costs. The poor reliability is in part due to utilization of the electrolytic capacitors that while providing the necessary high energy density and dI/dt rating,

have a limited life that decays rapidly under high current and temperature stresses [69]. As the active filters are scaled to higher voltages and power, the cost scales non-linearly due to the inclusion of step-up transformers, larger filters, sensors, and switching devices of higher ratings, and DC capacitors of higher energy densities. While there are companies that have commercialized active filters at low voltages, they are not widely employed at higher voltages.

The active filters can be configured in either shunt or series, as depicted in Figure 2.16. The shunt configuration is utilized for suppressing harmonics in the current, while the series configuration is employed for decoupling the voltage harmonics from the grid, thereby preventing interference with sensitive loads. Since this work is focused on the shunt or current-based compensations, the configuration shown in Figure 2.16(a) is considered.



(a) Shunt connected (b) Series connected

Figure 2.16: Shunt- and series-connected active filters for harmonic current and voltage compensation, respectively.

The operating principle of the shunt active filter is conceptually quite simple. The load current, $i_{LD} = i_S + i_H$, is sensed, where i_S is the fundamental component and i_H is the sum of all the undesired harmonics in the load current. Through digital signal processing, the individual harmonic components are extracted from i_H. For a three-phase, three-wire system, the triplen harmonics do not exist, so the lowest undesired harmonic is the 5th.

Generally, three-phase diode-rectified loads produce negative sequence harmonics at $h = 6n-1$ and positive sequence at $h = 6n+1$, where $n = [1, 2, 3, ..]$. In single-phase

systems, harmonics can potentially exist at every odd multiples of the fundamental line frequency.

The VSI generates currents at each harmonic frequency in anti-phase with the load harmonics such that: $i_{AF} = -i_H$. Therefore, the current generated by the VSI cancels out the harmonics in the load current, leaving the line current a clean sinusoidal at the fundamental frequency.

An example VSI harmonic controller operating in the synchronous reference frame and suppressing the 5th and the 7th harmonics is depicted in Figure 2.17. In this example, the harmonics are sensed from the line currents instead of the load currents. Synchronous reference frame transformations are applied to extract the DQ (DC) equivalents of the two harmonic frequencies. These DC terms are driven to zero with integrators. The outputs of the integrators go through inverse transformations to revert back to stationary reference frame. The results from each harmonic loop in the stationary reference frame are then summed together to generate the reference duty command for synthesizing the voltage that would subsequently drive the active filter current, $i_{AF} = -i_H$.

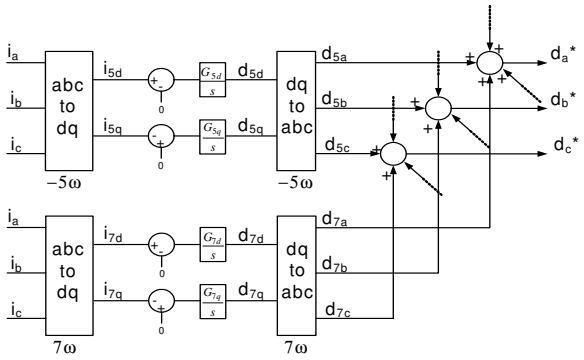


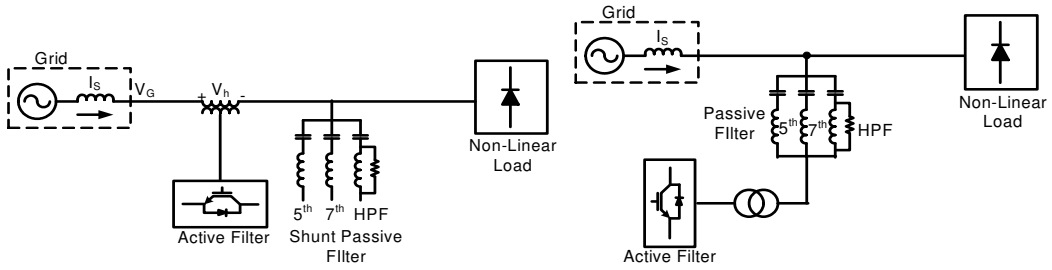
Figure 2.17: Example control architecture of a VSI-based active filter.

While it is technically feasible to combine VAR compensation and active filtering in one unit, this is typically not a standard practice due to the large ratings requirements of devices and components that can inflate the cost of the unit. It is rare or

impossible to find a STATCOM installation where the harmonic filtering functionality is included, as the cost justification for harmonic filtering at the medium-voltages has not been well made for these excessively expensive and rarely installed units. Conversely, active filters targeted for industrial applications have rarely been designed with power factor correction, as the cost of such a product would be comparable to installing an active front-end rectifier.

2.4.2.2 Hybrid Active Filters

Hybrid active filters are an alternate solution to the pure passive filters and the pure active filters that address their relatively high installation and operating costs. The hybrid topologies employ passive filters in combination with a fractionally-rated active topology, typically an inverter. Two different implementations of the hybrid active filters are shown in Figures 2.18(a) and 2.18(b) for series and shunt compensation, respectively.



(a) Series active, shunt passive (b) Shunt active and passive

Figure 2.18: Hybrid filters based on combination of active and passive components.

In low-voltage applications, the active component of the hybrid active filters are typically 10 percent of the rating of the pure active filters [1].

The operating principle of the hybrid active filters is similar to the passive filters with performance comparable to the pure active filters. While the passive filters are similarly tuned to individual harmonics, the active circuit only suppresses resonances and decouples the grid dynamics from overloading the passive filters [1, 7].

An example controller published in [1] is depicted in Figure 2.19. The controller is designed to provide a low impedance path for the 5th harmonic current using a feedforward control. Here, the DQ components of the 5th harmonic are extracted from the load current, i_L, and the 5th harmonic voltage reference is calculated for synthesizing the low-impedance path.

The feedback controller ensures that enough energy is drawn from the line to replenish the energy in the DC capacitor lost to internal losses, a feature that is common in all VSI-based VAR and harmonic compensators. Based on the harmonics present in the line current, i_S, the feedback controller synthesizes appropriate voltages to present a high impedance path to those same harmonics through the hybrid active filter, and thus preventing the series passive filters from overloading.

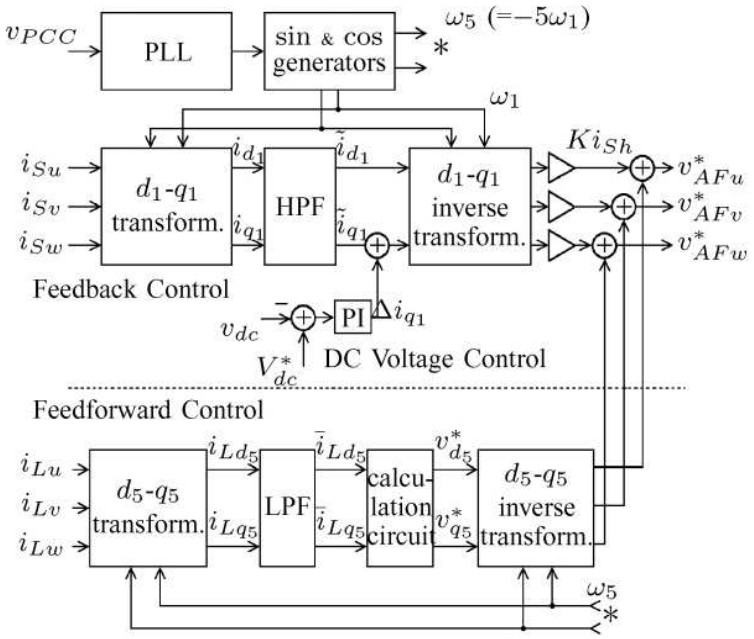


Figure 2.19: Example controller for low-voltage hybrid active filters for sinking fifth harmonics from the load while preventing harmonics and resonances in the line from overloading the passive filter [1].

The hybrid active filters provide an alternative approach to scaling to medium voltages because the active circuit only experiences fraction of the full line voltage.

Therefore, they are deemed to be more cost-effective than the pure active filters. But even then, market penetration has been very poor due to the necessity of step-up transformers or more complex multi-level VSI topologies, and complexity in the design of the passive components. Further, electrolytic capacitors are still utilized, limiting the life of the overall system, as well as requiring temperature-controlled environment similar to batteries.

2.5 Understanding the Market Needs

2.5.1 Benefits of Reactive Power Technologies

Quantifying economic benefits of the reactive and harmonic compensation technologies is a difficult endeavor. Capturing the benefits in mitigating the loss of productivity and maintaining system stability through prevention of blackouts and brownouts, improving operation and increasing the available transfer capacity of the system, regulating voltages to curb system losses and maintain stability margins, and etc., and attributing these benefits to a specific VAR and harmonic compensation unit installed at a particular location is not feasible. The difficulty in modeling the value proposition is further aggravated within a meshed network.

A few simplified real and hypothetical business cases can be examined in an attempt to quantify the economic benefits of reactive power compensation [48]:

- **Power Factor Correction:** TVA requires its distribution members to regulate the power factor between 0.95-1.00 in their substations. A charge of $1.46/kVAR-month for lagging and $1.14/kVAR-month for leading power factors are penalized against utilities that do not conform to this standard. The average power factor at Lenoir City Utilities Board (LCUB) was below the standard for up to four months in the period spanning August 2004 to July 2005, with values as low as 0.92 for the month of July. Through installation of 5 MVAR of reactive power compensation, the LCUB can avoid power factor

penalty charges of $29.2k/year, or an equivalent annual benefit of $5,840 per MVAR of compensation, expressed as **$5,840/MVAR-year**.

- **Decreased Line Losses:** A single line connecting a generator to a remote load center accrues 30 kW of losses per 1 MW of power transferred at a power factor of 0.9 for four months of the year without any compensation. By improving the power factor to 0.95 through VAR compensation, and subsequently reducing the losses by 10.3%, or 3.09 kW, an equivalent savings of **$2,853/MVAR-year** is realizable. Here, the average cost of electricity is assumed to be $50/MWh during the peak hours.

- **Increased Line Capacity:** For the same single-line scenario carrying 1 MW of power, by improving the power factor to 0.95, transfer capacity can also be increased by 5.2 percent, assuming the voltages at both ends remain the same. If the locational margininal pricing (LMP) differential between the generation and the remote load center is $5/MWh, which is a realistic price difference when comparing big cities and their neighboring areas, benefits of **$4,801/MVAR-year** is realizable.

Addressing harmonic pollutions is also critical to optimal and efficient operation of the power system as they can cause:

- Voltage distortion in distribution feeders.
- Increased RMS current leading heating and line losses.
- Overheating of power transformers.
- Derating of distribution equipment.
- Overloading of phase and neutral currents (neutral may even carry more current than the RMS phase).

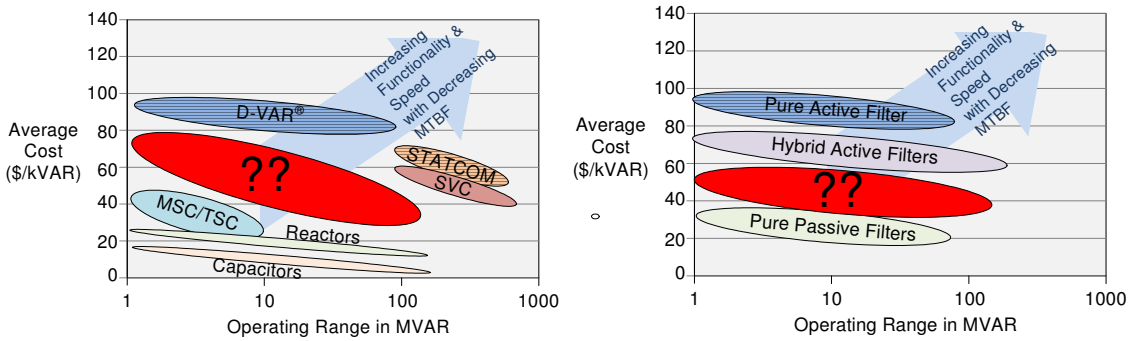
- Series and parallel resonances between utility and non-linear load leading to amplification of harmonic current.
- Overloading and fuse blowing of PFC capacitors.
- Tripping of voltage harmonic sensitive equipment.
- Failure of control electronics and micro-processors.
- Reduced accuracy of measurement equipment.
- Malfunction of solid-state fuses, breakers, and relays.
- High failure rate of filter capacitor banks.
- Reactive power and resonance problems.
- Reduced system stability and safe operating margins.

The business case for providing VAR and harmonic compensation ultimately depends on the cost-benefit analyses by the individual utility companies and their customers, which in turn depends on the geographic location, financial operating margins and discount rates, available interest rates, capital cost, and O&M cost of the specific compensation technology. The business practices and the financial drivers of the individual utility companies and their customers are beyond the scope of this work. However, the cost, the functionality and the typical ratings of the commercially available VAR and harmonic compensation technologies are considered in this work to identify the gaps in the market that a new technology could potentially capture.

2.5.2 Market Opportunities

There are segments of the market that clearly have not been addressed by the commercially available reactive power and harmonic filtering technologies discussed in the previous sections. The various reactive power technologies are plotted in terms

of their average installed cost and typical ratings in Figure 2.20(a). A similar plot for harmonic filtering technologies is given as well in Figure 2.20(b) with estimated installed costs. Both these plots identify gaps in the existing market, denoted by the ellipse with the question marks, where the potential to make a significant impact exists with a new technology.



(a) Reactive power technologies

(b) Harmonic filter technologies

Figure 2.20: The average cost of commercially available reactive power and harmonic filtering technologies in terms of capacity. The hashed background denotes inability to source unbalanced compensation for the indicated cost range.

A modular and a scalable technology that can provide VAR and harmonic compensation at a low cost, over a wide range of voltages and power ratings, with a long life, a relatively high performance metrics in terms of low THD, rapid sub-cycle response, and effectiveness in mitigating unwanted resonances and harmonics, can disrupt the existing market. A technology that can source unbalanced reactive power is also highly desirable, as much of the faults that occur on the grid are asymmetrical in nature. The cost range plotted in the figure for the more functional compensation technologies such as the STATCOM and D-VAR are for three-phase implementations that are limited in sourcing unbalanced VARs.

The poor reliability, the limited life, and the high capital cost have significantly limited the market penetration of the STATCOMs, even at high power ratings where the costs generally scale down. For example, installation of a 500 MVAR STATCOM

at $60/kVAR translates to a capital requirement of $30M, which is no easy task for any utility to justify for a single project where the return-on-investment (ROI) is often not very clear. American Superconductor attempted to address these limitations through the commercialization of the modular D-VAR system that can be installed incrementally with an 8 MVA building block. But the costs remain relatively high with their applications limited to the wind industry where the cost-benefits are better justified in certain geographic locations and where alternate solutions are even more expensive.

2.5.3 Utility Requirements

The failure rates and the limited life of the inverter-based solutions are the other two reasons that have also kept the utility companies away from the STATCOMs.

While the responsibility of deploying harmonic filters have historically fallen to the industrial customers with a large harmonic signature, the presence of harmonics in the distribution grid from unclassified single-phase loads are of increasing concerns to the utility companies as well. The present inverter-based harmonic filters are not adequately reliable while the passive filters are not robust and flexible enough to compensate the dynamic loads and sources on the grid. For the utilities to consider integrating a new piece of technology into their existing systems with reliability measured in multiple nines (99.999..%), the technology itself has to demonstrate high reliability in turn. The challenges are significant in developing a low-cost product with the following operating specifications that are typical of most grid assets:

- Long life of over 30 years.
- Outdoor installations with ambient temperature range of -40 to +55 degrees Celsius.
- Compact and modular packaging.

- High insulation clearances.
- High dI/dt and dV/dt ratings.
- Addressing issues related to fatigue from thermal cycling.
- Effective passive thermal management.
- Basic insulation level (BIL) to handle lightning strikes
- Differences in operating temperatures of the switching devices and the control electronics.

No existing VAR and/or harmonic compensation technology has been able to completely meet both the market needs and operating specifications of a conventional grid asset.

2.6 Current and Future Methods to Recover Costs

For load-serving entities (LSEs) or electricity distribution companies (EDCs), reactive power support through static capacitors or load tap changers are a normal part of the distribution network planning and operation. The costs are accounted in the utility's rate base, with fixed and variable costs recovered via retail rates applied to the customers served.

Within the PJM and MISO region, generators are paid based on cost-based schedule, Schedule 2, as approved by FERC, that are set in advance for reactive power support. The generator must be under the control of the ISO and be dispatchable to supply or absorb reactive power as needed.

Transmission owners who supply reactive power do not qualify for Schedule 2, even if they are using the lowest cost and the most effective approach compared to the generator-based compensation. Instead, they can rate base their investments upon approval of their retail regulators.

ISOs/RTOs like ISO-NE, PJM, and NYISO are attempting to create a more level playing field by applying principles of consistent compensation for similar supply types. Their objective is a single and a consistent compensation approach for all types of reactive power technologies, which would replace the generator-specific Schedule 2 now in effect. They are also trying to incentivize location-based pricing where lower system losses are encountered if the reactive support is located closer to the loads, as well as reduce prices for areas with lower requirements for reactive support.

Until more competitive compensation schemes are established and with compensation requirements existing mostly at the distribution levels closer to the load pockets, the burden of providing reactive support to support new load growth falls to the LSEs. Therefore, a low-cost compensation solution is critical for supporting load growth without noticeably impacting the cost of electricity paid by the end-use customers.

On the source side, the cost of providing reactive compensation to the intermittent renewable sources such as wind farms is accounted in the installed and/or operating costs of the renewable technology. By utilizing a technology with performance in par with STATCOMs but at the cost of TSRs, reliable integration of renewables with a low levelized cost of energy can be realized.

2.7 Conclusions

In the industrial and the utility-grid applications requiring dynamic VAR compensation, the MSCs, the TSCs, and the TSRs are the most widely adopted solutions. This is due to their low cost, driven partly by their relative simplicity in implementation as well as their modular approach to scaling in power. For these reasons, utility companies generally prefer the SVCs, built using TSRs and either static capacitors or MSCs, over the STATCOMs, despite the much greater functionality provided by the STATCOMs. Their simplicity also leads to their high reliability and low failure

rates, critical features in most grid applications. However, the high level of harmonics induced in the TSRs require large filters. Step-up transformers are also used in connecting the low-voltage modules to the grid. These requirements significantly increase the footprint of their installations, making them unsuitable in highly congested areas. As the TSRs are generally operated at low switching frequencies and harmonics generated are in the audible range, noise can also become problematic. These factors make it difficult to install the SVCs locally near big cities where VAR compensations are needed.

To realize the superior benefits of the STATCOMs at a smaller, lower-cost package, American Superconductor commercialized a technology called D-VAR that scales from low to high power in a modular fashion. However, the cost remains high, restricting applications to grid integration of wind energy where the cost-benefits are more justifiable.

Three-phase implementations of STATCOMs are limited in their capabilities to provide unbalanced compensation. This is a significant limitation as most faults that occur on the grid are asymmetrical in nature and therefore require unbalanced compensation. To address this drawback, AREVA developed a single-phase implementation called a Chain-Link STATCOM®. The downside of the single-phase implementations is a 10-fold increase in the energy storage requirements of the DC capacitors and subsequent increase in the cost of the system.

The poor reliability of the VSI-based technologies has also prevented the wider adoption of the STATCOMs. The primary failure mechanisms in inverters can be attributed to:

- The failures of the electrolytic capacitors through aging, drying out of the electrolytic solution, and high current stresses [36].
- The failures of the semiconductor switches due to aging, defects, or unexpected stresses.

- The failures of the thermal management system due to leakage of coolant or breakdown of fans and pumps.

Semiconductor device technologies are continually maturing and with that, their reliability, efficiency, and manufacturing yield rates continue to increase.

Such has not been the case with electrolytic capacitors where the technology has more or less fully matured at its present cost points. Companies such as Electronic Concepts have attempted to commercialize alternatives to the electrolytic capacitors under the brand name Unlytic^{TM} with a dry construction based on a film-based dielectric. These new capacitors offer performance superior to the electrolytic capacitors with a 10-fold increase in current density, a 3-fold increase in over-voltage protection, extended operating temperature range from -55 to 105 degrees Celsius, and with a 10-year shelf-life. But the costs of these Unlytics are 5 to 10 times higher, in terms of dollars per farad, and the energy densities are 40 to 50 times lower, in terms of joules per cubic-inch, than their electrolytic counterparts [25]. In the end, VAR and harmonic compensators that entirely obviate the requirement for bulk energy storage elements are much more desirable.

By designing converters of high efficiencies, the burden placed on the thermal management system can be slashed significantly. Lower losses translate to simpler thermal management requirements. Engineers have traditionally turned to "soft-switching" solutions to cut down switching losses and subsequently increase power densities. But these solutions typically require dramatically larger devices with high voltage and/or current ratings, which inflate the cost of the power conversion system. A solution that can realize high efficiencies with minimal device ratings can lead to systems that are not only smaller, but are also less costly and more reliable.

The matrix converter offers an alternative to VSIs in direct AC power conversion applications [87, 42, 44, 50, 60]. The concept is sound in theory but faces serious limitations in implementations that have delayed its commercialization. To date,

Yaskawa^{TM} is the only major company that manufactures the matrix-based motor drives. These limitations include higher device counts compared to back-to-back VSIs, complex or insufficient protection under faults, and errors in current and/or voltage measurements that lead to improper device commutations and subsequently to large spikes in the absence of polarized snubbers. Further, without any bulk energy storage in the converter itself, the converter requires all three phases to be present at the input to synthesize voltage waveforms of arbitrary magnitude, phase, and/or frequency on the output. The strong coupling and the dependence between the input phases pose serious limitations for applications requiring VAR and harmonic compensation, especially with unbalanced grid conditions and asymmetrical supply of reactive power.

A solution that can leverage the direct AC conversion functionality of the matrix converter to eliminate the use of the electrolytic capacitors entirely but one that is implemented on a single-phase basis; a solution that is able to provide the dynamic performance of the STATCOMs, realize low cost of the TSRs and the TSCs, and the reliability of static capacitors; such a solution can positively disrupt the existing market for VAR and harmonic compensation.

CHAPTER III

DYNAMIC VAR AND HARMONIC COMPENSATORS

3.1 Introduction

When a direct AC converter (DACC), comprised of an AC chopper circuit and small LC components for suppressing switching noise, as shown in Figure 3.1, is combined with a passive component, such as a resistor, an inductor, or a capacitor, the impedance of that particular component is dynamically controllable. In other words, a passive element is imbued with variable characteristics, as exemplified by Figure 3.2. This concept is similar to the thyristor-switched reactor (TSR) used in SVCs, where the firing angle effectively modifies the impedance of the inductor and thereby controls the magnitude of the injected inductive current. However, because the DACC utilizes fast switching IGBTs, it is able to respond to commands within a 1/10th of a cycle and does so without injecting any undesired low-frequency harmonics. In Figure 3.1, the AC chopper is functionally represented with a single-pole-double-throw (SPDT) switch, which is a four-quadrant switch that can carry current in both directions and block bi-polar voltages.

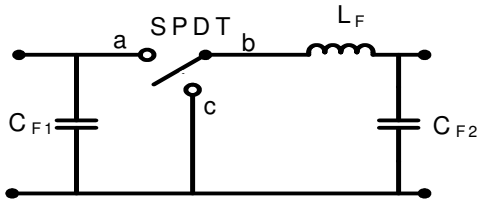


Figure 3.1: A direct AC converter (DACC) circuit.

The DACC is configurable as a buck, a boost, or a buck-boost circuit. These three classical topologies are extensively employed in DC-DC converter applications, and

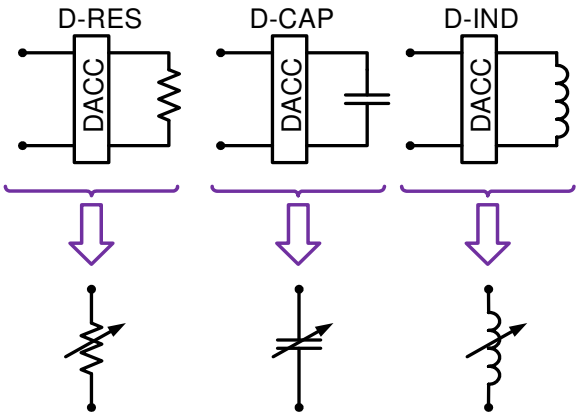


Figure 3.2: A static passive element is imbued with variable characteristics when interfaced with a DACC.

aside from the buck-boost topology, are also heavily used in DC-AC applications in the forms of voltage source inverters (VSIs) and current source inverters (CSIs).

For ease of reference, this dissertation will henceforth refer to the DACC interfaced with a resistor as a Dynamic Resistor (D-RES), with an inductor as a Dynamic Inductor (D-IND), and with a capacitor as a Dynamic Capacitor (D-CAP). While the D-RES is an interesting concept where a resistive element is used to provide harmonic compensation, it is unable to provide any VAR compensation at the fundamental frequency. Therefore, it will be briefly analyzed for its harmonic compensation capability. The other two classes of topologies fall under the family of Dynamic VAR and Harmonic Compensators (DVHC). Since applications requiring lagging or inductive VARs are very few, mostly confined to compensating for capacitive charging of high-voltage lines, the primary focus of this work is on the D-CAP.

Potential retrofit applications for this approach are vast where a DACC can be applied to shunt reactors, like the one shown in Figure 3.3(a), or to a bank of power factor correction capacitors such as the one shown in Figure 3.3(b) to augment them with cost-effective dynamic capabilities.

Realizing a variable impedance through PWM control is not a novel concept [18, 39]. However, such a concept has not seen practical applications in the industrial and

(a) Shunt reactor (b) PFC capacitors

Figure 3.3: Potential grid assets suitable for retrofit applications to enable dynamic characteristics.

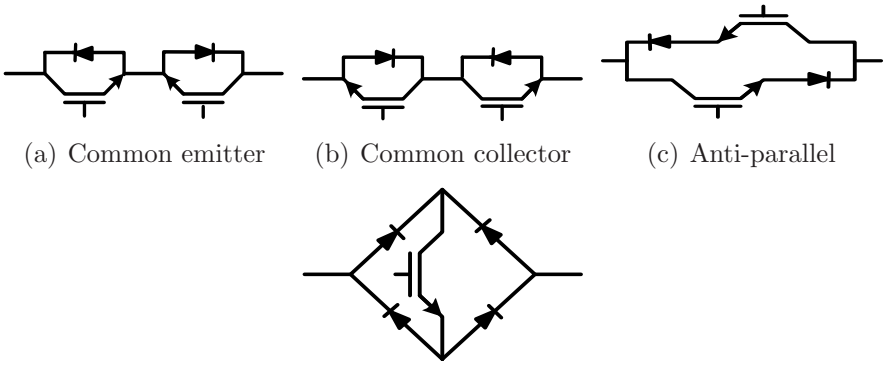
utility domains until more recently. For example, it has been shown that the buck and the boost DACC interfaced with film-VAR capacitors can dynamically inject leading VARs to regulate the voltage and support optimal grid operation [21]. And by applying the concept of virtual quadrature sources (VQS) [24], harmonics can be filtered simultaneously as well, a concept not thought possible in grid applications without using VSIs [19, 67].

This research work is based on the fundamental principles established in [19], and attempts to further that work by thoroughly analyzing and modeling the operation of the class of converters introduced here as the DVHCs. Further, practical implementations and controls in low- and medium-voltages are presented, along with simulation and experimental validations.

3.2 Implementations of the DVHCs

The four-quadrant single-pole-double-throw (SPDT) switch of Figure 3.1 is implemented using AC or bi-directional switches that conduct current and block voltage in both directions. There are essentially four different approaches to realizing an AC switch using IGBTs or MOSFETs, as depicted in Figure 3.4. Selection of an

appropriate configuration is based on trade-offs between cost, performance, and commercial availability. For this work, configurations shown in Figure 3.4(a) and Figure 3.4(b) are selected due to their superior control and performance, as well as ready availability of the individual IGBT modules with integrated anti-parallel diodes.



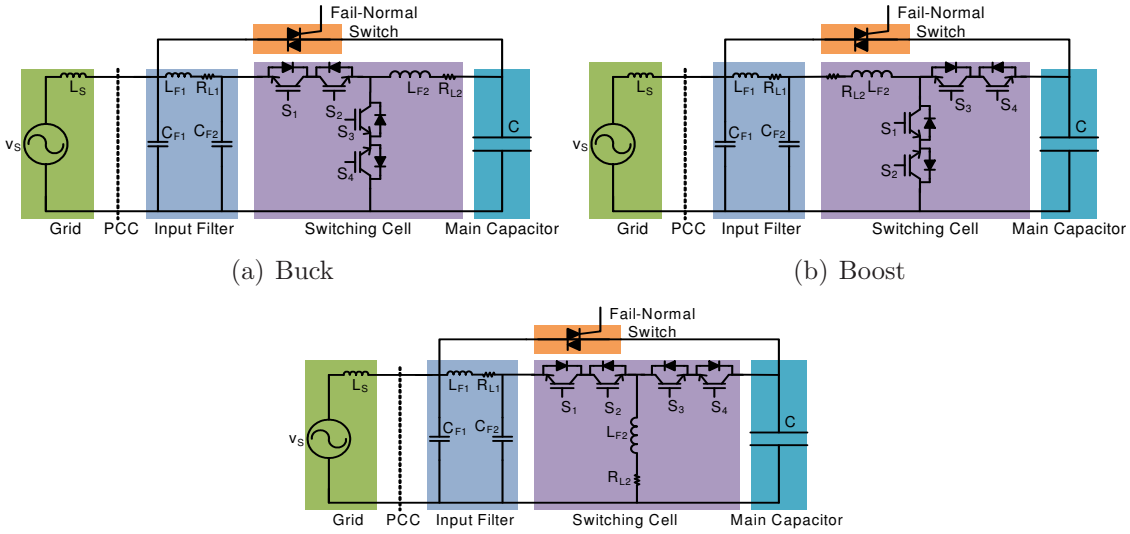
(a) Common emitter (b) Common collector (c) Anti-parallel

(d) Diode bridge

Figure 3.4: The four different implementations of an AC switch.

The three two-level D-CAP configurations with input filters are shown in Figure 3.5. Similar implementations of the D-IND and the D-RES are given by Figures 3.6 and 3.7, respectively. The two IGBT switch-pairs, S_1/S_2 and S_3/S_4, are the two AC switches to provide the four-quadrant operation of the converter. The component, L_{F2}, is the primary switching inductor, facilitating the conversion of voltages and currents. A third-order input filter is depicted in each of the nine circuits and is comprised of the components, C_{F1}, C_{F2}, and L_{F1}. A filter of a different order or topology may be utilized per total harmonic distortion (THD) requirements of the design.

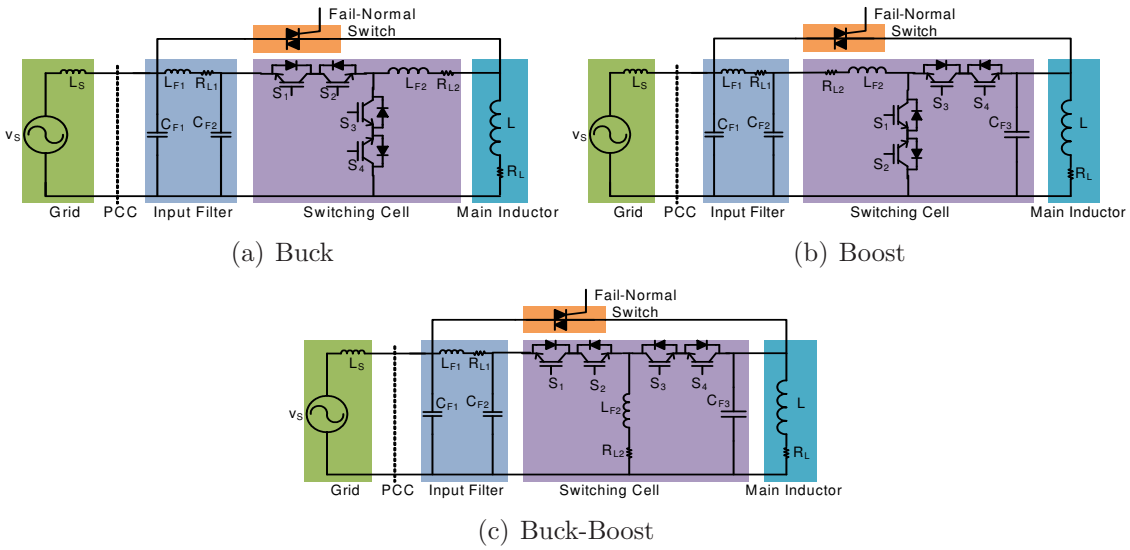
The converters are seen interfacing the grid at the point of common coupling, or PCC, which is defined by IEEE 519 as a common "interface between sources and loads," and where compensation is most beneficial. In this work, the utility-grid is modeled as an ideal voltage source in series with an impedance set by the inductor, L_S.



(a) Buck (b) Boost

(c) Buck-Boost

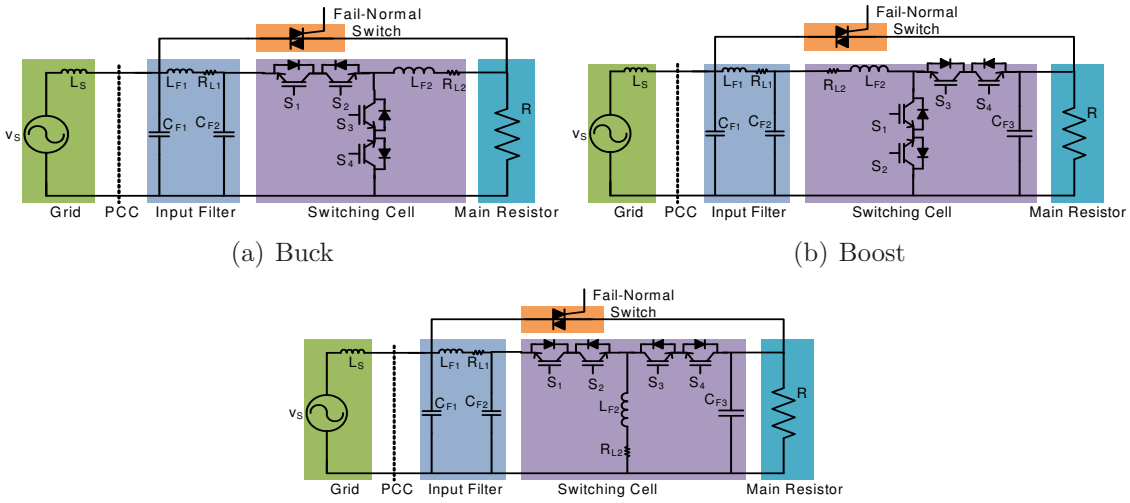
Figure 3.5: The three configurations of the Dynamic Capacitor.



(a) Buck (b) Boost

(c) Buck-Boost

Figure 3.6: The three configurations of the Dynamic Inductor.



(a) Buck

(b) Boost

(c) Buck-Boost

Figure 3.7: The three configurations of the Dynamic Resistor.

While the figures only demonstrate single-phase DVHCs, they can be applied to both single- and three-phase applications. In three-phase systems, because of the single-phase implementation, unbalanced and asymmetrical compensation can be sourced, a feature wholly lacking in a three-phase VSI without dramatic oversizing of the DC capacitor.

A slight disadvantage of the boost and buck-boost configurations for the D-IND and D-RES is that an additional capacitor, C_{F3}, is also required for energy buffering to maintain current continuity for the D-IND and voltage buffering for the D-RES.

A "fail-normal" switch comprised of a thyristor-pair ensures that when the converter fails, it can be bypassed, so that the original functionality of the asset is restored. For high-power applications, thyristors of low ratings may be paralleled with a mechanical switch to reduce the cost of fully rated thyristors. The mechanical switch takes several line cycles to activate, during which time the thyristors can be quickly turned on to provide a short-term bypass. Thyristors have a surge rating that can be leveraged to provide this functionality. The fail-normal approach preserves the reliability of the grid asset. Such a characteristic is very attractive in utility-grid

applications.

3.3 Dynamic VAR Injection

The ideal converter gains of the classical DC-DC converters are directly applicable for the presented buck, boost, and buck-boost AC converters and are given as follows:

$$M = \begin{cases} d(t) & \text{for the buck,} \\ \frac{1}{1-d(t)} & \text{for the boost,} \\ \frac{d(t)}{1-d(t)} & \text{for the buck-boost,} \end{cases} \tag{3.1}$$

where

$$\begin{aligned} d(t) &\equiv \text{duty cycle of the switches } S_1 \text{ and } S_2, \\ 1-d(t) &\equiv \text{duty cycle of the switches } S_3 \text{ and } S_4, \\ d(t) &\in [0,1]. \end{aligned} \tag{3.2}$$

These ideal gains are derived under the assumption that there are no parasitics in the converter and the voltage drops across the filter elements are negligible.

Based on these gains, Table 3.1 lists the equivalent impedance as a function of the constant duty cycle, $d(t) = K_0$, of the switches for all nine circuits of Figures 3.5-3.7. These expressions indicate that by controlling the duty cycle of the switches, the effective resistance, capacitance, or inductance connected at the PCC can by dynamically varied. With inductors and capacitors, the proposed converters can provide dynamic VAR compensation with performance, in terms of response and spectral contents, at par with the VSI-based STATCOMs.

3.3.1 Idealized Operating Domains

An ideal VAR compensator is able to provide a constant 1 pu of fundamental reactive current for a range of line voltages, even under unbalanced conditions. By taking the three impedance equations for the buck, the boost, and the buck-boost D-CAP from

Table 3.1: The dynamic impedance of the three passive components when interfaced with the three DACC configurations and operated with a constant duty cycle, $d(t) = K_0$.

Configurations	Resistor (Ω)	Capacitor (Ω)	Inductor (Ω)
Buck	$\frac{1}{K_0^2}R$	$\frac{1}{K_0^2}\frac{1}{j\omega C}$	$\frac{1}{K_0^2}j\omega L$
Boost	$K_0^2 R$	$K_0^2\frac{1}{j\omega C}$	$K_0^2 j\omega L$
Buck-Boost	$\frac{(1-K_0)^2}{K_0^2}R$	$\frac{(1-K_0)^2}{K_0^2}\frac{1}{j\omega C}$	$\frac{(1-K_0)^2}{K_0^2}j\omega L$

Table 3.1, the following expressions for the fundamental reactive current are obtained:

$$I_{DCAP} = \begin{cases} K_0^2 I_C & \text{for the buck,} \\ \frac{1}{K_0^2} I_C & \text{for the boost,} \\ \frac{K_0^2}{(1-K_0)^2} I_C & \text{for the buck-boost,} \end{cases} \tag{3.3}$$

where

$$I_C = V_S \omega C e^{j\frac{\pi}{2}} \equiv \text{three-phase reactive power rating of C,}$$

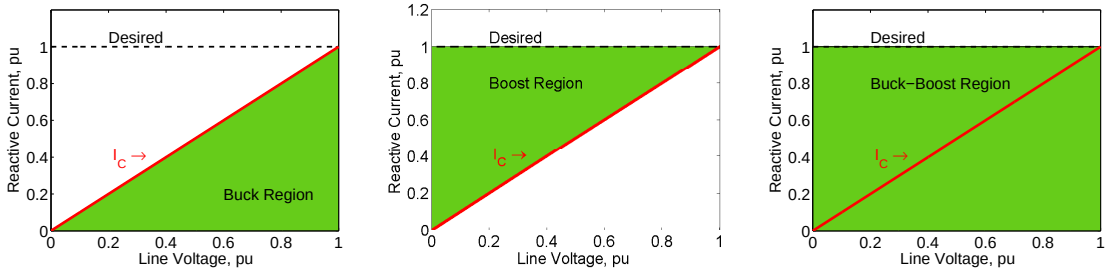
$$V_S \equiv \text{grid line-to-neutral voltage,}$$

$$\omega \equiv \text{fundamental line frequency in rad/s,}$$

$$C \equiv \text{main capacitor's value.}$$

Based on these expressions, the ideal operating domain of the three topologies are given by the plots in Figure 3.8. The dashed line marked "Desired" describes the characteristic of an ideal VAR compensator where the said unit is able to inject 0 to 1 pu of VAR current for any given line voltage. Of the three configurations, only the ideal buck-boost is able to operate within the full span of this domain. Both the ideal buck and the boost topologies are limited in their operating domains, where the buck is only able to operate in the domain below the trajectory of a fixed capacitor it is interfacing with, while the boost can only operate above that same trajectory.

The individual limitation of the buck and the boost is addressable by paralleling them together, such that together, they encompass the same operating domain as the buck-boost. Another more limiting but potentially less costly alternative is to design the buck unit such that the 1 pu "Desired" operating line goes partially through its operating domain. This is achieved by oversizing the devices and components in the buck topology such that it is able to inject above 1 pu of reactive power.



(a) Buck (b) Boost (c) Buck-Boost

Figure 3.8: The ideal operating regions of the three D-CAP configurations juxtaposed with the desired reactive current reference of an ideal STATCOM, given as a dashed line, and current injected by a capacitor, I_C.

The operating domains are further limited by device and component ratings, parasitics, filter and system impedances, and losses. Operating domains under realistic conditions are discussed in Chapter 4.

The system-level impact of the buck and the boost for supporting the grid voltage is shown in Figure 3.9 for select nodes in an example IEEE 34-node system [74]. The simulated results validate that the D-CAP is much more effective than simple capacitors.

3.4 Active Harmonic Filtering

By modulating the AC switches in a particular manner, controllable odd harmonic currents can be synthesized to cancel out the harmonics generated by the neighboring loads and measured at the PCC. To realize this functionality, the concept of VQS is employed [24].

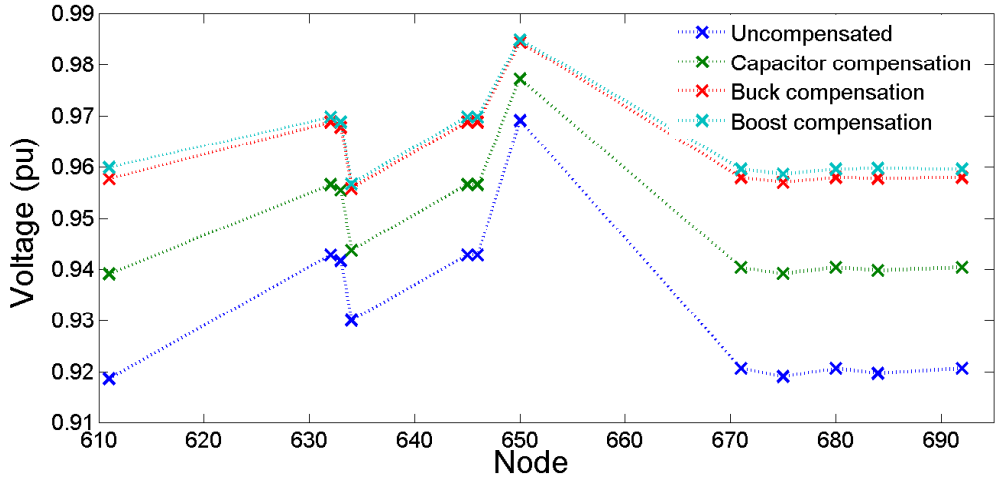


Figure 3.9: Simulated impact of VAR compensation on the voltage profile of an example IEEE 34-node system with a buck and a boost D-CAP in comparison with a capacitor.

3.4.1 Principle of Virtual Quadrature Sources

In a VSI, the DC source in conjunction with the AC line voltages are used to synthesize arbitrary voltages across the output filter inductors, which based on the voltage impressed across them, will drive currents with the desired harmonic components, as exemplified by Figure 3.10.

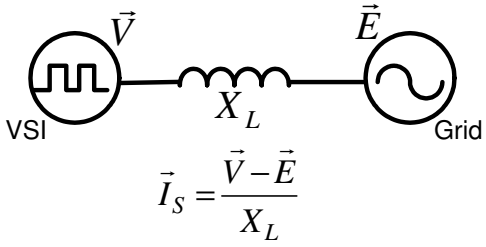


Figure 3.10: The voltage, V, is synthesized based on the desired current,I_S, in a VSI.

This research takes an alternate approach where only the AC source is used to synthesize an arbitrary AC waveform across a passive component with a direct AC converter. The passive component, in turn, generates a current, which is then reflected

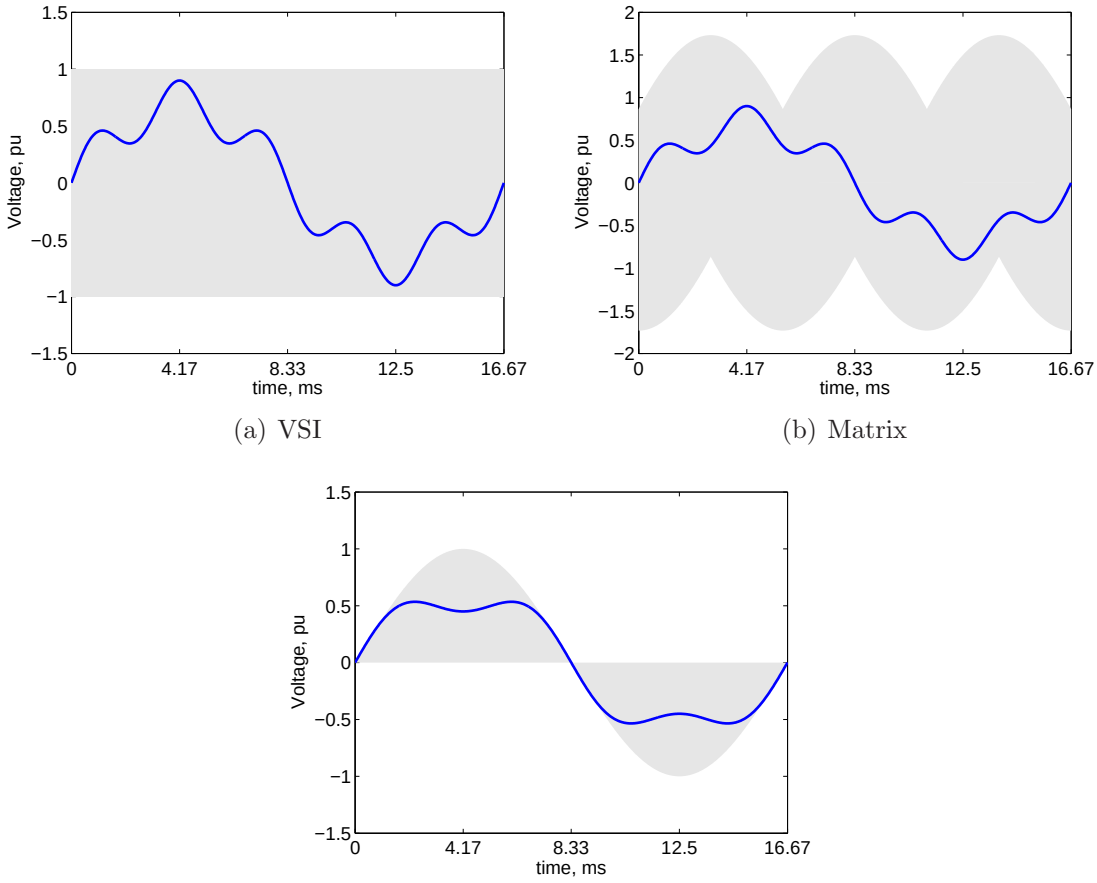
back through the converter to the source side. The waveform synthesized across the passive component is controlled based on the desired current to be injected back into the AC source. Therefore, unlike a VSI, which behaves as a two-port network with voltage sources on both sides, the proposed concept behaves more like a one-port device.

Synthesis of any arbitrary voltage or current is possible as long as the synthesized waveform is within the envelope of the input source(s). Synthesized voltage is confined within the $\pm V_{DC}$ band in a VSI, as shown in Figure 3.11(a). The matrix converter synthesizes an arbitrary voltage within the combined envelope of its three-phase sources in Figure 3.11(b). The available envelope for synthesizing waveforms for DVHCs with a single sinusoidal AC source is given by Figure 3.11(c).

With a single-phase AC source as the input, the available voltage decays to zero at $\phi = n\pi$ angles. Attempting to synthesize a voltage outside of this sinusoidal envelope is not possible without additional energy. For that reason, to synthesize a particular waveform that is even partially outside of the sinusoidal envelope, other components that are orthogonal to the desired ones must also be synthesized simultaneously, such that the summation of all the individual components fall within the input envelope. This concept is exemplified by Figure 3.12, where the desired component is the phase-shifted fundamental waveform marked 'filtered output' whose synthesis is not possible without the addition of a third harmonic component. In effect, the energy exchange in this example is occurring between three "virtual" sources, namely the two orthogonal waveforms at the fundamental frequency and one at the third harmonic, in order for the desired waveform to exist outside of the envelope.

3.4.2 Example Syntheses of the 5th and 7th Harmonics

In a balanced three-phase, three-wire system, the first two harmonics that requires filtering are typically the 5th and the 7th. However, synthesizing only these two



(a) VSI

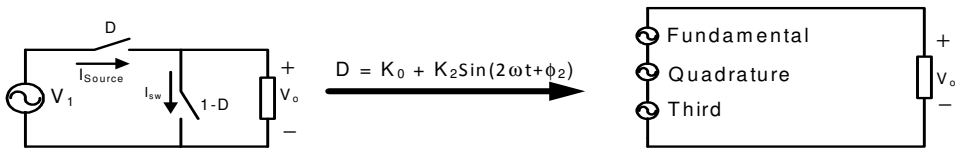
(b) Matrix

(c) DVHC

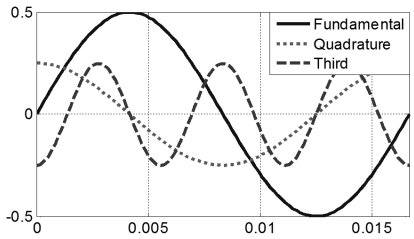
Figure 3.11: The envelopes within which arbitrary voltages may be synthesized in a VSI, a matrix converter, and a DVHC.

harmonic components with an AC chopper interfaced to a single AC source is not possible as the sum of these two arbitrary voltages have segments that reside outside of the source envelope, as shown in Figure 3.13. Other orthogonal quantities have to be synthesized as well such that there is energy available to generate the 5th and the 7th harmonics.

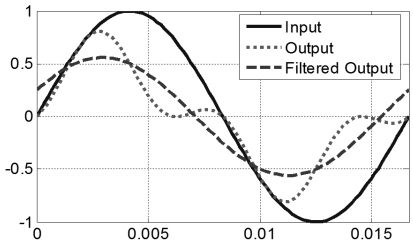
For an AC chopper topology, because the envelope is not mirrored over the $y = 0$ axis, a component at the fundamental frequency is required. After including a fundamental component, the waveform lies mostly within the source envelope in Figure 3.14. A third harmonic component with a particular phase is also introduced. The



(a) Generation of VQS terms through modulation of the AC switches



(b) Components of the synthesized output voltage



(c) Fundamental output lies outside the envelope of the input

Figure 3.12: Synthesis of an output voltage that lies outside the envelope of the input voltage through the concept of VQS.

resulting waveform is now completely inside the envelope in Figure 3.15.

While the fundamental and third harmonic components were not initially targeted, they do not take away from the value of the concept. The fundamental component is useful because it allows the grid asset to dynamically serve its original functionality - a key feature for providing VAR injection with the D-CAPs and the D-INDs. Whereas the third harmonic component, because the system is assumed to be a three-wire system, is canceled naturally when it sums with the third harmonic components generated by the other two phases of the unit. The third harmonic component becomes more useful for filtering in four-wire or single-phase systems.

The synthesized voltage contains components that are orthogonal to each other, since the real power exchanged between the sources of different frequency is zero, and because these harmonics are virtual and not real, the term "virtual quadrature sources" is used.

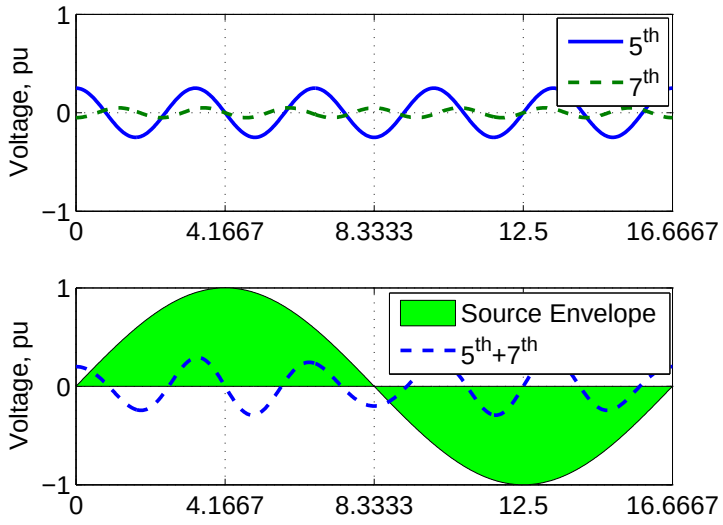


Figure 3.13: Synthesis of a waveform with the 5th and the 7th harmonic components lying outside the envelope of the input source.

3.4.3 Even Harmonic Modulation (EHM)

The switch duty-cycle function in the DVHC takes on a particular form to generate the necessary VQS terms for harmonic filtering. The derivation of such a function is

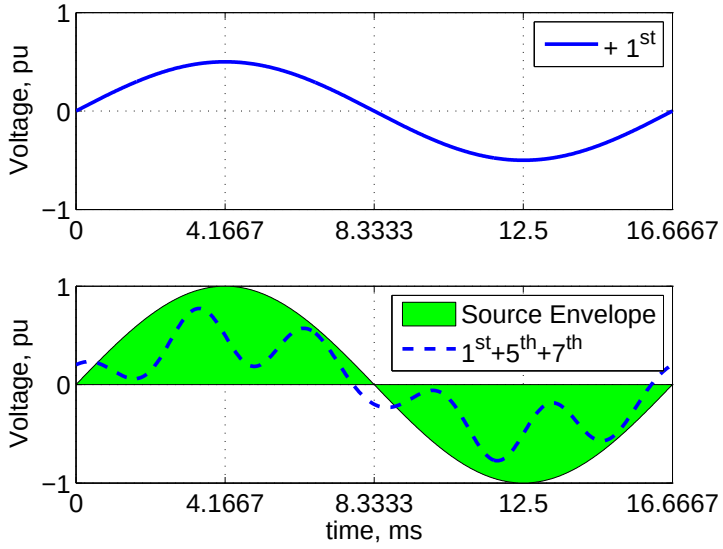


Figure 3.14: Synthesis of a waveform with the 5th, the 7th, and the 1st harmonic components lying mostly inside the envelope of the input source.

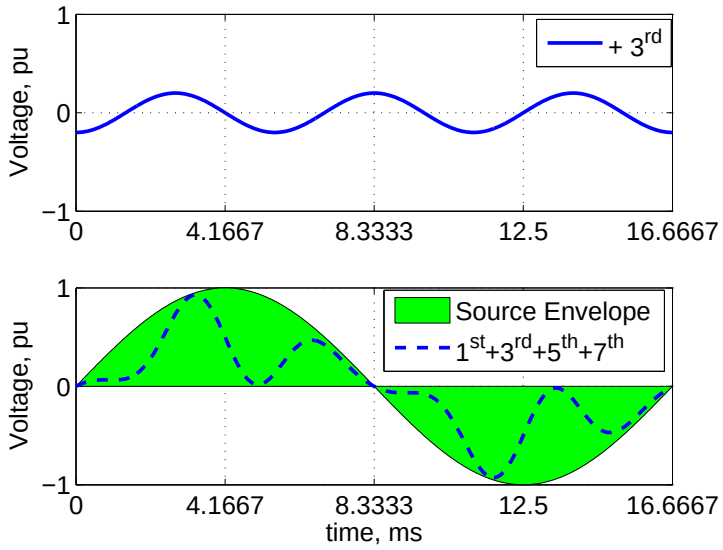


Figure 3.15: Synthesis of a waveform with the 5th, the 7th, the 1st, and the 3rd harmonic components lying completely inside the envelope of the input source.

explored in this section.

In an active filter based on the VSI topology, the reference duty function is derived as:

$$\begin{aligned} d(t) &= \frac{V_o^*}{V_{in}} \\ &= \{V_1 \sin(\omega t) + V_3 \sin(3\omega t + \phi_3) \\ &\quad + V_5 \sin(5\omega t + \phi_5)\} / V_{DC} \\ &= (K_1) \sin(\omega t + \phi_1) + (K_3) \sin(3\omega t + \phi_3) \\ &\quad (K_5) \sin(5\omega t + \phi_5) + ..., \end{aligned} \tag{3.4}$$

where the numerator is the desired voltage on the output, and denominator or the input is the DC voltage. The constant term in the denominator leads to a very simple expression for the duty cycle.

For the DVHCs, the voltages and currents are synthesized from an AC source instead, so the denominator is sinusoidal. The duty expression for an AC chopper in

a buck configuration is derived as follows:

$$d(t) = \frac{V_o^*}{V_m \sin(\omega t)} \tag{3.5}$$

$$= K_0 + K_2 \sin(2\omega t + \phi_2) + K_4 \sin(4\omega t + \phi_4) + ..., \tag{3.6}$$

where V_o^* contains the fundamental and the odd harmonic terms for VAR and harmonic compensation. As it is not clear what restrictions have to be in place for the harmonic terms in V_o^*, in order for the output voltage to lie inside the envelope of the input voltage, the expression for V_o^* is derived by multiplying the input voltage with the duty cycle, instead of starting with the desired output voltage and then trying to derive the duty cycle. Solving for V_o^* in Equation (3.6) leads to the following expression:

$$\begin{aligned} V_o^* = {} & K_0 V_m \sin(\omega t) + \frac{K_2 V_m}{2} \cos(\omega t + \phi_2) \\ & - \frac{K_2 V_m}{2} \cos(3\omega t + \phi_2) + \frac{K_4 V_m}{2} \cos(3\omega t + \phi_4) \\ & - \frac{K_4 V_m}{2} \cos(5\omega t + \phi_4) + ... \end{aligned} \tag{3.7}$$

Because the duty cycle contains sinusoidal terms at even harmonics of the fundamental, the scheme is termed "even harmonic modulation" or EHM. The EHM scheme synthesizes VQS and was derived after many trial-and-error iterations where different expressions for duty cycle were considered that would generate the desired fundamental and odd harmonic components. The K_0 term in Equation (3.6) is the constant duty cycle used in AC choppers for scaling the input voltage, while the sinusoidal terms lead to the generation of $n\omega \pm 1$ side bands. For the n-th harmonic voltage impressed across the network of passive components, the network will draw current at the same harmonic frequency. After the current is reflected over the AC switches, it is tuned to cancel out the harmonics generated by the nearby loads.

3.4.4 Application of VQS for Harmonic Compensation

In order to cancel out the harmonic currents generated by the non-linear loads, the active filter injects current at the same frequency and amplitude but in anti-phase with the load harmonics. This filter is typically connected in shunt, as shown in Figure 3.16. In contrast, active filters for compensating voltage disturbance on the grid and decoupling the load from the grid dynamics are typically connected in series. The DACC when interfaced with a transformer is known as a controllable network transformer (CNT) [20]. When the CNT is controlled using the concept of VQS, it has the potential to provide the series harmonic compensation. The DVHCs of this work are not suitable for series compensation.

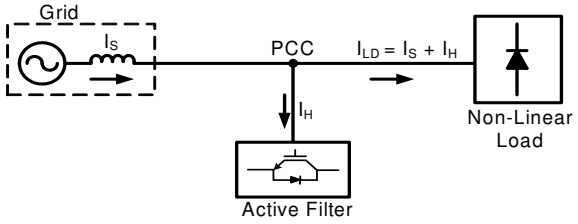


Figure 3.16: An active filter connected in shunt to suppress undesired harmonic currents in the load from propagating into the grid.

3.4.4.1 Harmonic Filtering Using the Buck Configuration

Using the buck configuration as an example, the switches are modulated with the duty function,

$$d(t) = K_0 + K_2 \sin(2\omega t + \phi_2) + K_4 \sin(4\omega t + \phi_4), \tag{3.8}$$

for the grid voltage given by,

$$V_S(t) = V_m \sin(\omega t). \tag{3.9}$$

The subsequent current generated by the buck D-RES is then:

$$I_{DRES}(t) = d(t)^2 \frac{V_S(t)}{R} \tag{3.10}$$

$$= I_{\omega}(t) + I_{3\omega}(t) + I_{5\omega}(t) + I_{7\omega}(t) + I_{9\omega}(t),$$

where

$$\begin{aligned} I_{\omega}(t) = \frac{1}{2}\frac{V_m}{R}\{&\left(2K_0^2 + K_2^2 + K_4^2\right)\sin(\omega t) \\ &+2K_0K_2\cos(\omega t + \phi_2) \\ &-K_2K_4\sin(\omega t - \phi_2 + \phi_4)\}, \end{aligned} \tag{3.11}$$

$$\begin{aligned} I_{3\omega}(t) = \frac{1}{4}\frac{V_m}{R}\{&-4K_0K_2\cos(3\omega t + \phi_2) \\ &+K_2^2\sin(3\omega t + 2\phi_2) \\ &+4K_0K_4\cos(3\omega t + \phi_4) \\ &+2K_2K_4\sin(3\omega t - \phi_2 + \phi_4)\}, \end{aligned} \tag{3.12}$$

$$\begin{aligned} I_{5\omega}(t) = \frac{1}{4}\frac{V_m}{R}\{&-4K_0K_4\cos(5\omega t + \phi_4) \\ &+K_2^2\sin(5\omega t + 2\phi_2) \\ &+2K_2K_4\sin(5\omega t + \phi_2 + \phi_4)\}, \end{aligned} \tag{3.13}$$

$$\begin{aligned} I_{7\omega}(t) = \frac{1}{4}\frac{V_m}{R}\{&-2K_2K_4\sin(7\omega t + \phi_2 + \phi_4) \\ &+K_4^2\sin(7\omega t + 2\phi_4)\}, \end{aligned} \tag{3.14}$$

$$I_{9\omega}(t) = -\frac{1}{4}\frac{V_m}{R}\left\{K_4^2\sin(9\omega t + 2\phi_4)\right\}. \tag{3.15}$$

Similar derivations result in the current for the buck D-IND:

$$\begin{aligned} I_{DIND}(t) &= \frac{d(t)}{L}\int d(t)\, V_S(t)\, dt \\ &= I_{\omega}(t) + I_{3\omega}(t) + I_{5\omega}(t) + I_{7\omega}(t) + I_{9\omega}(t), \end{aligned} \tag{3.16}$$

where

$$\begin{aligned} I_{\omega}(t) = \frac{1}{30}\frac{V_m}{\omega L}\{&-30K_0^2\cos(\omega t) \\ &+5K_2^2\cos(\omega t) \\ &+K_4^2\cos(\omega t)\}, \end{aligned} \tag{3.17}$$

$$
\begin{aligned}
I_{3\omega}(t) = \frac{1}{60}\frac{V_m}{\omega L}\{&-40K_0K_2\sin(3\omega t+\phi_2)\\
&-15K_2^2\cos(3\omega t+2\phi_2)\\
&-20K_0K_4\sin(3\omega t+\phi_4)\\
&+12K_2K_4\cos(3\omega t-\phi_2+\phi_4)\},
\end{aligned}
\tag{3.18}
$$

$$
\begin{aligned}
I_{5\omega}(t) = \frac{1}{60}\frac{V_m}{\omega L}\{&-36K_0K_4\sin(5\omega t+\phi_4)\\
&+5K_2^2\cos(5\omega t+2\phi_2)\\
&-20K_2K_4\cos(5\omega t+\phi_2+\phi_4)\},
\end{aligned}
\tag{3.19}
$$

$$
\begin{aligned}
I_{7\omega}(t) = \frac{1}{60}\frac{V_m}{\omega L}\{&8K_2K_4\cos(7\omega t+\phi_2+\phi_4)\\
&-5K_4^2\sin(7\omega t+2\phi_4)\},
\end{aligned}
\tag{3.20}
$$

$$
I_{9\omega}(t) = \frac{1}{60}\frac{V_m}{\omega L}\left\{K_4^2\sin(9\omega t+2\phi_4)\right\}, \tag{3.21}
$$

and for the buck D-CAP,

$$
\begin{aligned}
I_{DCAP}(t) &= d(t)\,C\frac{d}{dt}\left[d(t)\,V_S(t)\right] \\
&= I_\omega(t)+I_{3\omega}(t)+I_{5\omega}(t)+I_{7\omega}(t)+I_{9\omega}(t),
\end{aligned}
\tag{3.22}
$$

where

$$
I_\omega(t) = \frac{1}{2}V_m\omega C\left\{\left(2K_0^2+K_2^2+K_4^2\right)\cos(\omega t),\right. \tag{3.23}
$$

$$
\begin{aligned}
I_{3\omega}(t) = \frac{1}{4}V_m\omega C\{&8K_0K_2\sin(3\omega t+\phi_2)\\
&+K_2^2\cos(3\omega t+2\phi_2)\\
&-4K_0K_4\sin(3\omega t+\phi_4)\\
&+4K_2K_4\cos(3\omega t-\phi_2+\phi_4)\},
\end{aligned}
\tag{3.24}
$$

$$
\begin{aligned}
I_{5\omega}(t) = \frac{1}{4}V_m\omega C\{&12K_0K_4\sin(5\omega t+\phi_4)\\
&+3K_2^2\cos(5\omega t+2\phi_2)\\
&+4K_2K_4\cos(5\omega t-\phi_2+\phi_4)\},
\end{aligned}
\tag{3.25}
$$

$$I_{7\omega}(t) = \frac{1}{4}V_m\omega C\left\{-8K_2K_4\sin(7\omega t+\phi_2+\phi_4)\right. \\ \left.+3K_4^2\cos(7\omega t+2\phi_4)\right\}, \tag{3.26}$$

$$I_{9\omega}(t) = -\frac{5}{4}V_m\omega C\left\{K_4^2\cos(9\omega t+2\phi_4)\right\}. \tag{3.27}$$

These derivations do not take into account the parasitics and assume the voltage drops across the switching filter components are negligible.

Observation of these expressions reveal that the injected currents are comprised of a component at the fundamental frequency as well as components at odd multiples of the fundamental frequency. The fundamental component provides fulfillment of the asset's original functionality but now augmented with dynamic capabilities. The odd harmonic components can be tuned to cancel out the harmonics injected at the PCC by dirty loads.

The difficulty in controlling any individual harmonic is clearly obvious, as there are multiple parameters of the EHM terms affecting any particular odd harmonic current. Modeling and control techniques are presented in the later chapters of this work that provide guidance on understanding how exactly DVHCs should be operated and controlled as harmonic filters.

3.4.4.2 Ideal Converter Gains with Even Harmonic Modulation

The individual harmonic components for the boost and buck-boost topologies are difficult to separate analytically. This is due to the presence of multi-frequency sinusoidal terms in the denominator of the gain function of these two switching cells, as given by,

$$M_{boost} = \frac{1}{1-d(t)}, \tag{3.28}$$

for the boost and,

$$M_{buck-boost} = \frac{d(t)}{1-d(t)}, \tag{3.29}$$

for the buck-boost. This is unlike the case for the buck where,

$$M_{buck} = d(t) = \underbrace{K_0}_{\text{Constant}} + \underbrace{K_2 \sin(2\omega t + \phi_2) + K_4 \sin(4\omega t + \phi_4) + \ldots}_{\text{Even Harmonic}}. \tag{3.30}$$

In order to validate that the EHM-based duty function, originally derived using a buck configuration, is still applicable in generating the VQS terms with the boost and buck-boost configurations, the switching gains have to be resolved to the EHM form given by Equation (3.30).

Taylor series approximation is employed in linearizing the gain expression for the boost and buck-boost. The general form of the Taylor series representation relevant to this discussion is:

$$\frac{x^m}{1-x} = \sum_{n=m}^{\infty} x^n \qquad \text{for: } |x| < 1 \text{ and } m \in N_0 \tag{3.31}$$

The gain function for the boost with up to the 4th even harmonic term in the duty function, $d(t)$, is considered and is rewritten as follows:

$$M_{boost} = \frac{1}{1-K_0} \frac{1}{1 - \left(\frac{K_2}{1-K_0} \sin(2\omega t + \phi_2) + \frac{K_4}{1-K_0} \sin(4\omega t + \phi_4) \right)} \tag{3.32}$$

$$= \frac{1}{1-K_0} \frac{1}{1-y} \tag{3.33}$$

Representing the expression as a power series,

$$M_{boost} = \frac{1}{1-K_0} \sum_{n=0}^{\infty} y^n, \tag{3.34}$$

where

$$y = \frac{K_2}{1-K_0} \sin(2\omega t + \phi_2) + \frac{K_4}{1-K_0} \sin(4\omega t + \phi_4). \tag{3.35}$$

Here, Taylor series is used to represent the function, M_{boost}, with an infinite sum of the power series of y. Since $|y| < 1$, the higher order terms are assumed to be negligible and the gain function is approximated with up to the second order term as:

$$M_{boost} \cong \frac{1}{1-K_0} \left(1 + y + y^2\right) \tag{3.36}$$

Substituting for y, expanding the trigonometric powers as a sum of harmonics, and collecting the terms based on their harmonic number, the following expression is obtained:

$$M_{boost} = \underbrace{M\left(0\right)}_{\text{Constant}} + \underbrace{M\left(2\omega\right) + M\left(4\omega\right) + M\left(6\omega\right) + M\left(8\omega\right)}_{\text{Even Harmonic}}, \tag{3.37}$$

where

$$M\left(0\right) = \frac{1}{1-K_0} + \frac{1}{2}\frac{K_2^2}{\left(1-K_0\right)^3} + \frac{1}{2}\frac{K_4^2}{\left(1-K_0\right)^3}, \tag{3.38}$$

$$\begin{aligned} M\left(2\omega\right) = {} & \frac{K_2}{\left(1-K_0\right)^2}\sin\left(2\omega t + \phi_2\right) + \frac{1}{2}\frac{K_2K_4}{\left(1-K_0\right)^3}\cos\left(-2\omega t + \phi_2 - \phi_4\right) \\ & + \frac{1}{2}\frac{K_2K_4}{\left(1-K_0\right)^3}\cos\left(2\omega t + \phi_4 - \phi_2\right), \end{aligned} \tag{3.39}$$

$$M\left(4\omega\right) = \frac{K_4}{\left(1-K_0\right)^2}\sin\left(4\omega t + \phi_4\right) - \frac{1}{2}\frac{K_2^2}{\left(1-K_0\right)^3}\cos\left(4\omega t + 2\phi_2\right), \tag{3.40}$$

$$M\left(6\omega\right) = -\frac{K_2K_4}{\left(1-K_0\right)^3}\cos\left(6\omega t + \phi_2 + \phi_4\right), \tag{3.41}$$

$$M\left(8\omega\right) = -\frac{1}{2}\frac{K_4^2}{\left(1-K_0\right)^3}\cos\left(8\omega t + 2\phi_4\right). \tag{3.42}$$

This approximation for the boost's gain function is clearly equivalent to the EHM form given by Equation (3.30), where the effective gain is comprised of a constant term plus even harmonic terms. Therefore, applying this expression results in the generation of currents with a fundamental term plus odd harmonic terms, similar to the buck case in Equations (3.11)-(3.27). No further analyses are required to validate the harmonic filtering capability of the boost DVHCs.

Similar approximation is carried out for the buck-boost configuration. The power series of the gain function is derived as follows:

$$\begin{aligned} M_{buck-boost} = {} & \frac{K_0}{1-K_0}\frac{1}{1-\left(\frac{K_2}{1-K_0}\sin\left(2\omega t + \phi_2\right) + \frac{K_4}{1-K_0}\sin\left(4\omega t + \phi_4\right)\right)} \\ & + \frac{\frac{K_2}{1-K_0}\sin\left(2\omega t + \phi_2\right) + \frac{K_4}{1-K_0}\sin\left(4\omega t + \phi_4\right)}{1-\left(\frac{K_2}{1-K_0}\sin\left(2\omega t + \phi_2\right) + \frac{K_4}{1-K_0}\sin\left(4\omega t + \phi_4\right)\right)} \end{aligned} \tag{3.43}$$

$$= \frac{K_0}{1-K_0}\frac{1}{1-y} + \frac{y}{1-y} \tag{3.44}$$

Representing as power series,

$$M_{buck-boost} = \frac{K_0}{1-K_0}\sum_{n=0}^{\infty} y^n + \sum_{n=1}^{\infty} y^n \tag{3.45}$$

$$\cong \frac{1}{1-K_0}\left(K_0 + y + y^2 \underbrace{+y^3}_{\text{added}}\right), \tag{3.46}$$

where

$$y = \frac{K_2}{1-K_0}\sin\left(2\omega t + \phi_2\right) + \frac{K_4}{1-K_0}\sin\left(4\omega t + \phi_4\right). \tag{3.47}$$

The Taylor series approximation of the buck-boost gain function is very similar to the boost, except for the K_0 factor in the constant term that is not present in the expression for the boost and the additional y factor that leads to the added term, y^3. Not including the additional y^3 term, by expanding the trigonometric powers and collecting the individual harmonics, the following expression is obtained:

$$M_{buck-boost} = \underbrace{M\left(0\right)}_{\text{Constant}} + \underbrace{M\left(2\omega\right) + M\left(4\omega\right) + M\left(6\omega\right) + M\left(8\omega\right)}_{\text{Even Harmonic}}, \tag{3.48}$$

where

$$M\left(0\right) = \frac{K_0}{1-K_0} + \frac{1}{2}\frac{K_2^2}{\left(1-K_0\right)^3} + \frac{1}{2}\frac{K_4^2}{\left(1-K_0\right)^3}, \tag{3.49}$$

$$M\left(2\omega\right) = \frac{K_2}{\left(1-K_0\right)^2}\sin\left(2\omega t + \phi_2\right) + \frac{1}{2}\frac{K_2K_4}{\left(1-K_0\right)^3}\cos\left(-2\omega t + \phi_2 - \phi_4\right) + \frac{1}{2}\frac{K_2K_4}{\left(1-K_0\right)^3}\cos\left(2\omega t + \phi_4 - \phi_2\right), \tag{3.50}$$

$$M\left(4\omega\right) = \frac{K_4}{\left(1-K_0\right)^2}\sin\left(4\omega t + \phi_4\right) - \frac{1}{2}\frac{K_2^2}{\left(1-K_0\right)^3}\cos\left(4\omega t + 2\phi_2\right), \tag{3.51}$$

$$M\left(6\omega\right) = -\frac{K_2K_4}{\left(1-K_0\right)^3}\cos\left(6\omega t + \phi_2 + \phi_4\right), \tag{3.52}$$

$$M\left(8\omega\right) = -\frac{1}{2}\frac{K_4^2}{\left(1-K_0\right)^3}\cos\left(8\omega t + 2\phi_4\right). \tag{3.53}$$

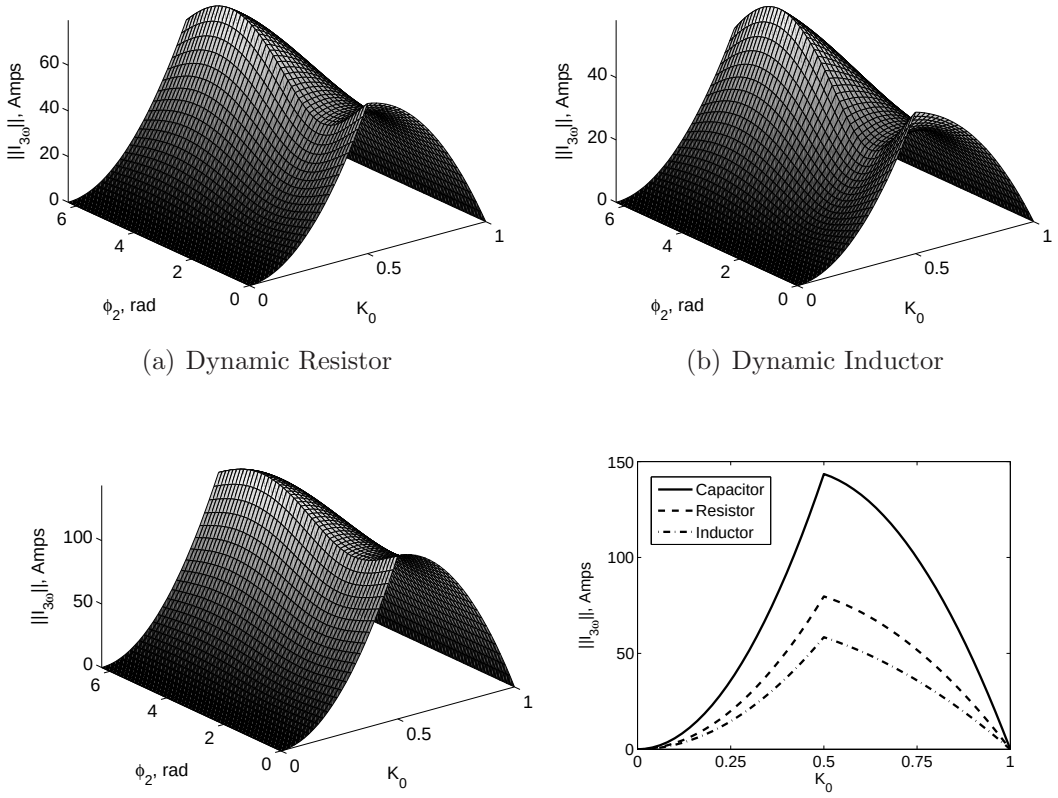
The final gain expression is truly identical to the boost case except for the additional K_0 in the constant term, $M(0)$. The differences in the constant terms in the boost and buck-boost gain functions make a significant impact upon the spectral content of the injected current. This can be directly observed from Equations (3.11)-(3.27), if the K_0 term in those current expressions are replaced by the $M(0)$ term from either the boost or buck-boost gain expressions.

Due to the presence of the additional y^3 term in the approximation of the buck-boost, which was not considered in the final derivation of the gain expression, undesired higher order harmonics are slightly more dominant. The lower order harmonics are influenced to a small degree as well. But because $|y| < 1$, per the assumption that led to the Taylor series approximation, the effect of y^3 term will not be very significant. Nevertheless, these harmonics will increase the overall THD of the buck-boost for the same input filter design.

3.4.5 Harmonic Characteristics of Passive Components

Each of the three passive elements have significantly different impedance as a function of frequency. An example case scenario is examined where the passive components are rated to provide 100 kVA per phase at 480 V/60 Hz, corresponding to a design of $R = 1.536\ \Omega$ for the D-RES, $L = 4.1$ mH for the D-IND, and $C = 1.7$ mF for the D-CAP. Considering only the constant and second even harmonic term in the duty function, the amount of third harmonic current injected by the three units are shown in Figure 3.17.

The plots clearly demonstrate that the D-CAP systems are much more effective in providing harmonic filtering for the same rating and control effort. This characteristic can be better understood by examining the relationship between the magnitude of the current drawn by each of the three types of passive elements in response to the



(a) Dynamic Resistor

(b) Dynamic Inductor

(c) Dynamic Capacitor

(d) Comparison at a constant ϕ_2

Figure 3.17: The magnitude of the third harmonic current drawn as a function of K_0 and ϕ_2 by the buck configured DVHCs with the resistor, the capacitor, and the inductor sized with their impedance equal to the base impedance of a 100 kVA system at 480 V / 60 Hz.

voltage with n-th harmonic component impressed across it, as given by:

$$\begin{aligned} \|I_R(n)\| &= \left|\tfrac{1}{R}V\right| \quad \propto \quad 1 && \text{for a resistor,} \\ \|I_C(n)\| &= |n\omega CV| \quad \propto \quad n\omega && \text{for a capacitor,} \\ \|I_L(n)\| &= \left|\tfrac{1}{n\omega L}V\right| \quad \propto \quad \tfrac{1}{n\omega} && \text{for an inductor.} \end{aligned}$$

A resistor will draw harmonic current with magnitude that is independent of the harmonic number itself. In contrast, the magnitude of the current drawn by a capacitor increases with increasing harmonic number, whereas, the magnitude of the current decreases with increasing harmonic number for inductors.

3.5 Conclusions

The underlying concept behind the class of Dynamic VAR and Harmonic Compensators is presented in this chapter. The concept is based on augmenting existing grid assets like a resistor, an inductor or a capacitor with a direct AC converter comprised of AC switches and small filter components, to realize the Dynamic Resistor, the Dynamic Inductor, and the Dynamic Capacitor, respectively. The direct AC converter can be configured as a buck, a boost, or a buck-boost to provide a suite of capabilities as needed by a particular application. The idealized characteristics of each configuration for providing VAR and harmonic compensation were explored.

A fail-normal switch bypasses the converter to preserve the assets original reliability if and when the converter should fail. This feature ensures that a single-point failure does not bring the whole system down, as it would in a STATCOM, but continues providing some level of limited compensation. The lack of bulk energy storage elements like the electrolytic capacitors in the converter also increases the overall reliability and reduces the burden on the thermal management system.

The input filter capacitor(s) used in suppressing switching harmonics also serves in a secondary role of supplying base reactive power required by the system. This inherent hybridization of static and dynamic capabilities realizes the optimal performance at the lowest cost, as the burden of providing the base reactive power requirements of the system are not penalized through higher device ratings. The devices can be rated exclusively for supplying that $\pm\Delta Q_{max}$ dynamic reactive power required by the system.

A constant duty-cycle control provides the full dynamic capability to adjust the supply of reactive power. This increases the robustness of the control system, as unlike a VSI, the reactive power can immediately be ramped up by slowly sweeping the duty from 0 to the nominal operating point, without going through complex initialization process where voltages have to be synchronized before compensation

can begin. The synchronization-less operation is due to the fact that there are no other 'sources' besides the grid itself. In a VSI, the presence of the DC source can cause large power oscillations if synchronization is lost due to a disturbance on the grid. With the DVHCs, as they are effectively modeled as variable impedances, there is never any danger of either losing synchronization or inducing power oscillations.

Using the recently developed concept of virtual quadrature sources (VQS), current harmonics in the grid and neighboring loads can be isolated and prevented from propagating onward and corrupting the voltages. This chapter demonstrated that even a resistor can be made to provide harmonic filtering. However, applications for the Dynamic Inductor and Dynamic Capacitors are more prevalent as they can provide both reactive power and harmonic compensation, simultaneously.

In a utility-grid environment, there is a great sensitivity to reliability and cost. Traditional power-electronics-based solutions such as STATCOMs have not been able to make much penetration into this very conservative market. The DVHC class of converters promises to provide similar performance as STATCOMs but with higher reliability and lower costs.

CHAPTER IV

TIME-DOMAIN MODELING

4.1 Introduction

In order to understand the transient and dynamic characteristics of the three D-CAP configurations, time-domain analytical and numerical expressions are derived in this chapter. The derivations take into account the effect of parasitic resistance and the switching inductance.

The input filters are not considered in the derivations as they are not critical to understanding the sub-switching transient behavior of the D-CAP. The input filter capacitors will supply additional reactive power at the fundamental frequency, but their contribution can be accounted as static capacitors that are connected in parallel to a grid with zero short-circuit impedance (ideal source). The input filter inductor is assumed to have negligible voltage drop across it at the harmonics well below the switching frequency.

The results are compared with simulation results of switching models. Unless specified otherwise, the switching models used in this work are based on ideal switches without any switching or conduction losses. These models are employed under the assumption that the inclusion of detailed physics model of the semiconductor devices make a negligible impact upon the overall behavior and control of the converter when operated in a manner described in this work. This is generally true if the rise and fall times of the devices are much smaller than their on or off time. Further, the forward voltage drops of the devices are assumed to be much smaller than the voltages being blocked by these devices.

The time-domain results are used to derive the operating regions of the buck,

boost, and the buck-boost D-CAP. The operating regions show the injected reactive current and losses versus duty or line voltage for different natural frequencies and different damping factors of the converter. Understanding how the various parameters affect the maximum injection capacity is critical to designing a high-performance D-CAP or D-IND.

4.2 Formulation of the Governing Equations

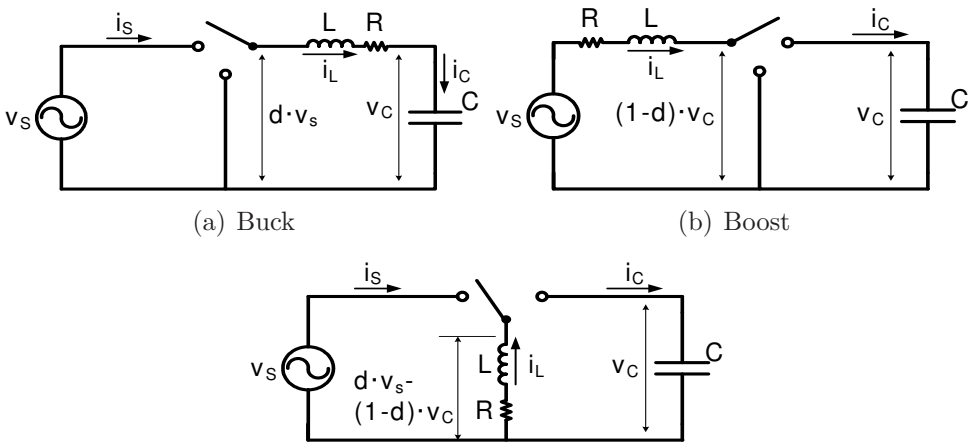
The simplified schematics of the AC buck, boost, and buck-boost topologies for realizing the D-CAP functionality are given by Figure 4.1 where the two AC switches are equivalently represented by a single-pole-double-throw (SPDT) switch. For each of these three topologies, under the assumption of high frequency synthesis, where $s(t) \Rightarrow d(t)$, and even harmonic modulation (EHM), the switch duty function takes on the following form:

$$d(t) = K_0 + K_2 \sin(2\omega t + \phi_2) + K_4 \sin(4\omega t + \phi_4) + ... \tag{4.1}$$

The constant term provides fundamental VAR injection while the even harmonic terms, which are multiples of the line fundamental frequency, provide harmonic filtering. To compensate for the n-th odd harmonic current in the grid, the $(n-1)$-th even harmonic term in the duty function is utilized. The logic behind this approach is discussed in Chapter 7.

Applying Kirchhoff's current and voltage laws, the following integro-differential equations with respect to time are derived that describe the behavior of the three configurations:

$$\frac{di_L(t)}{dt} + \frac{R}{L} i_L(t) + \frac{M_2}{LC} \int_0^t M_2 i_L(\tau)\, d\tau = M_1 \frac{1}{L} v_S(t), \tag{4.2}$$



(a) Buck (b) Boost

(c) Buck-Boost

Figure 4.1: The three configurations of the DACC drawn with a single-pole-double-throw switch.

where

$$M_1 = \begin{cases} d(t) \\ 1 \\ d(t) \end{cases} \qquad M_2 = \begin{cases} 1 & \text{for the buck,} \\ 1 - d(t) & \text{for the boost,} \\ 1 - d(t) & \text{for the buck-boost,} \end{cases}$$

$R \equiv$ parasitic resistance in series with inductor,

$L \equiv$ filter inductance,

$C \equiv$ main capacitor,

$d(t) \equiv$ time-varying duty cycle of the switches.

The buck configuration is used to exemplify the derivation of the analytical and numerical solutions to the integro-differential equation. While not explicitly shown, a similar approach is adapted in deriving the solutions for the other two configurations as well.

4.3 Analytical Solution for a Constant Duty Function

For purely fundamental VAR injection applications (i.e. STATCOM functionality), the operation of the converter is modeled with a constant duty control, $d(t) = K_0$.

Thus, differentiating the governing equation for the buck configuration with respect to time results in,

$$\frac{di_L^2(t)}{dt^2} + \frac{R}{L}\frac{i_L(t)}{dt} + \frac{1}{LC}i_L(t) = \frac{K_0}{L}\frac{d}{dt}v_S(t).$$

Applying Laplace transform and solving for $I_L(s)$ leads to:

$$I_L(s) = V_S(s)\,Y(s),$$

where

$$\begin{aligned} Y(s) &= \frac{K_0}{L}\frac{s}{s^2 + 2\alpha s + \omega_0^2}, \\ \alpha &= \frac{R}{2L}, \\ \omega_0 &= \frac{1}{\sqrt{LC}}. \end{aligned}$$

By applying inverse Laplace transform, the following time-domain, closed-form expressions for the inductor current for the different damping coefficients are obtained:

$$i_L(t) = \begin{cases} \frac{K_0}{L}\int_0^t v_S(t-\tau)\,e^{-\alpha\tau}\left(\cos(\omega_{ud}\tau) - \frac{\alpha}{\omega_{ud}}\sin(\omega_{ud}\tau)\right)d\tau & \text{for } \zeta < 1, \\ \frac{K_0}{L}\int_0^t v_S(t-\tau)\,e^{-\alpha\tau}(1-\alpha\tau)\,d\tau & \text{for } \zeta = 1, \\ \frac{K_0}{L}\int_0^t v_S(t-\tau)\,e^{-\alpha\tau}\left(\cosh(\omega_{od}\tau) - \frac{\alpha}{\omega_{od}}\sinh(\omega_{od}\tau)\right)d\tau & \text{for } \zeta < 1, \end{cases} \quad (4.3)$$

where

$$\begin{aligned} \omega_{ud} &= \sqrt{\omega_0^2 - \alpha^2}, \\ \omega_{od} &= \sqrt{\alpha^2 - \omega_0^2}, \\ \zeta &= \frac{\alpha}{\omega_0}. \end{aligned}$$

The primary variable of interest for the D-CAP is the source current, $i_S(t)$, as defined in Figure 4.1. For the buck configuration, this current is calculated by,

$$i_S(t) = K_0 i_L(t) \quad (4.4)$$

4.4 Numerical Solution for Non-Constant Duty Function

In applications where active harmonic filtering is required, where a constant duty cycle cannot be assumed, the integro-differential expression of Equation (4.2) can be represented numerically. The quadrature method is used to replace the integral term with a discretized expression as given by,

$$\int_a^b y(t) = \sum_{j=0}^{a} A_j y(t_j) + \epsilon_n(y),$$

where t_j, for $j = [0, 1, 2, ..., n]$, are the quadrature nodes,

$$A_j = \begin{cases} \frac{1}{2}h & \text{for} j = [0, n], \\ h & \text{for} j = [1, 2, \cdots, n-1], \end{cases}$$
$$h = \frac{b-a}{n},$$

n is the number of subintervals given by,

$$n = 2^m \in [a, b],$$

for $m \geq 2$ and,

$$\epsilon_n(y) \equiv \text{truncation error.}$$

Using finite difference method to discretize the derivative terms, the first- and the second-order differentiation are represented by,

$$\frac{dy}{dx}|_i \cong \frac{y(x_{i+1}) - y(x_{i-1})}{2h},$$
$$\frac{d^2y}{dx^2}|_i \cong \frac{y(x_{i+1}) - 2y(x_i) + y(x_{i-1})}{2h},$$

respectively. With these two sets of substitutions, the governing equation is solved numerically as follows:

$$i_L(t_{k+1}) = 2\Delta t \frac{1}{L} d(t_{k-1})\, v_S(t_{k-1}) + 2\Delta t \frac{1}{LC} \sum_{j=0}^{k-1} i_L(t_j) + \left(1 - 2\Delta t \frac{R}{L}\right) i_L(t_{k-1}) \quad (4.5)$$

In turn, the reflected source current is,

$$i_S\left(t_{k+1}\right) = d\left(t_{k+1}\right) i_L\left(t_{k+1}\right) + \epsilon_{k+1}\left(i_S\right). \tag{4.6}$$

4.5 Idealized Analytical Solution for Non-Constant Duty Function

In certain instances, especially when attempting to gain an insight into the circuit behavior, an expression can be simplified by eliminating higher order effects. In this case, the general behavior of the circuit can be described by neglecting the voltage drops across the switching filter elements and the parasitic components. The voltage drop across the equivalent resistor is assumed to be negligible based on,

$$Ri_L\left(t\right) << \frac{1}{C}\int_0^t i_L\left(\tau\right) d\tau,$$

and similarly, the voltage across the switching inductor is considered negligible from,

$$L\frac{di_L\left(t\right)}{dt} << \frac{1}{C}\int_0^t i_L\left(\tau\right) d\tau,$$

when compared with the voltage across the primary capacitor, C. These are valid assumptions when C is sized to be relatively much higher than the filter inductance, L, and the system is not very lossy. Based on these two assumptions, the following expression for the source current, $i_S\left(t\right)$, is found:

$$i_S\left(t\right) = d\left(t\right) C\frac{d}{dt}\left(d\left(t\right) v_S\left(t\right)\right) \tag{4.7}$$

The resulting expression does not make any assumptions on the form of the duty-cycle function, $d\left(t\right)$, thereby allowing the idealized expression to examine harmonic interactions when the converter is operated with the even harmonic modulation.

4.6 Generalization of the Solution-Sets

The analyses for the boost and buck-boost configuration are undertaken using an approach similar to the buck-configuration. The three solution-sets for each of the

three D-CAP configurations are aggregated and generalized with unique modulation parameters, thereby highlighting the similarities and differences between the three configurations.

An interesting noteworthy behavior in the analytical solution-set with a constant duty is that the natural frequency, ω_0, is significantly affected by the duty cycle of the switches in the boost and buck-boost case. This is because the capacitor, C, and the inductor, L, are separated by the switching cell that are modulated at the rate of $1-K_0$. As this is not the case for the buck configuration, its natural frequency is not affected by the switch modulation. This characteristic may destabilize the boost and buck-boost under a harmonic filtering operation when the natural frequency coincides with the harmonic frequency being filtered. Thus, the burden falls on the designer to ensure that the natural or characteristic frequency of the converter never coincides with the discrete harmonics that the D-CAP is trying to suppress. This caveat is valid for the buck configuration design as well.

4.6.1 Operation Under Constant Duty

The generalized solution-set under constant duty-cycle control in voltage support and power factor correction applications are given by,

$$i_S(t) = m_1 i_L(t), \tag{4.8}$$

where

$$i_L(t) = \begin{cases} \frac{m_1}{L}\int_0^t v_S(t-\tau)\, e^{-\alpha\tau}\left(\cos(\omega_{ud}\tau) - \frac{\alpha}{\omega_{ud}}\sin(\omega_{ud}\tau)\right)d\tau & \text{for } \zeta < 1, \\ \frac{m_1}{L}\int_0^t v_S(t-\tau)\, e^{-\alpha\tau}\,(1-\alpha\tau)\,d\tau & \text{for } \zeta = 1, \\ \frac{m_1}{L}\int_0^t v_S(t-\tau)\, e^{-\alpha\tau}\left(\cosh(\omega_{od}\tau) - \frac{\alpha}{\omega_{od}}\sinh(\omega_{od}\tau)\right)d\tau & \text{for } \zeta > 1, \end{cases}$$

$$\omega_{ud} = \sqrt{\omega_0^2 - \alpha^2}, \qquad \omega_{od} = \sqrt{\alpha^2 - \omega_0^2},$$

$$\zeta = \frac{\alpha}{\omega_0}, \qquad \alpha = \frac{R}{2L},$$

$$\omega_0 = \begin{cases} \frac{1}{\sqrt{LC}} \\ \frac{1-K_0}{\sqrt{LC}} \\ \frac{1-K_0}{\sqrt{LC}} \end{cases} \quad m_1 = \begin{cases} K_0 & \text{for the buck,} \\ 1 & \text{for the boost,} \\ K_0 & \text{for the buck-boost.} \end{cases}$$

4.6.2 Operation Under Even Harmonic Modulation

The generalized solution-set under non-constant duty-cycle control of the converters in VAR and harmonic compensation applications, which are represented numerically through discretization of the time-dependent variables, are given by,

$$i_S\left(t_{k+1}\right) = M_{1(k+1)} i_L\left(t_{k+1}\right), \tag{4.9}$$

where

$$i_L\left(t_{k+1}\right) = 2\Delta t \frac{1}{L} M_{1(k-1)} v_S\left(t_{k-1}\right) - 2\Delta t \frac{1}{LC} M_{2(k-1)} \sum_{j=0}^{k-1} M_{2(k-1)} i_L\left(t_j\right) + \left(1 - 2\Delta t \frac{R}{L}\right) i_L\left(t_{k-1}\right),$$

$$\begin{array}{llll} M_{1(k-1)} = d\left(t_{k-1}\right), & M_{2(k-1)} = 1, & M_{1(k+1)} = d\left(t_{k+1}\right) & \text{for buck,} \\ M_{1(k-1)} = 1, & M_{2(k-1)} = 1 - d\left(t_{k-1}\right), & M_{1(k+1)} = 1 & \text{for boost,} \\ M_{1(k-1)} = d\left(t_{k-1}\right), & M_{2(k-1)} = 1 - d\left(t_{k-1}\right), & M_{1(k+1)} = d\left(t_{k+1}\right) & \text{for buck-boost.} \end{array}$$

4.6.3 Idealized Operation Under Even Harmonic Modulation

The generalized solution-set under non-constant duty-cycle control of the converters in VAR and harmonic compensation applications, where the impact of filter elements and parasitics are neglected, are given by,

$$i_S\left(t\right) = MC \frac{d}{dt}\left(M v_S\left(t\right)\right), \tag{4.10}$$

where

$$M = \begin{cases} d(t) & \text{for buck,} \\ \frac{1}{1-d(t)} & \text{for boost,} \\ \frac{d(t)}{1-d(t)} & \text{for buck-buck.} \end{cases}$$

4.7 Accuracy of the Derived Expressions

To ascertain the models' accuracy, the numerical and the simplified analytical expressions for the non-constant duty function are compared with simulations results obtained from the switching models of the buck, the boost, and the buck-boost D-CAP on a 480 V / 60 Hz system. The comparisons are for configurations where $C = 1$ mF, $L = 100\mu$F, and $R = 0.1\Omega$. The switching frequency of the devices is set to 10 kHz. The duty function with up to the 4th even harmonic term for the buck and boost is,

$$d(t) = 0.5 + 0.05\sin(2\omega t) + 0.02\sin(4\omega t),$$

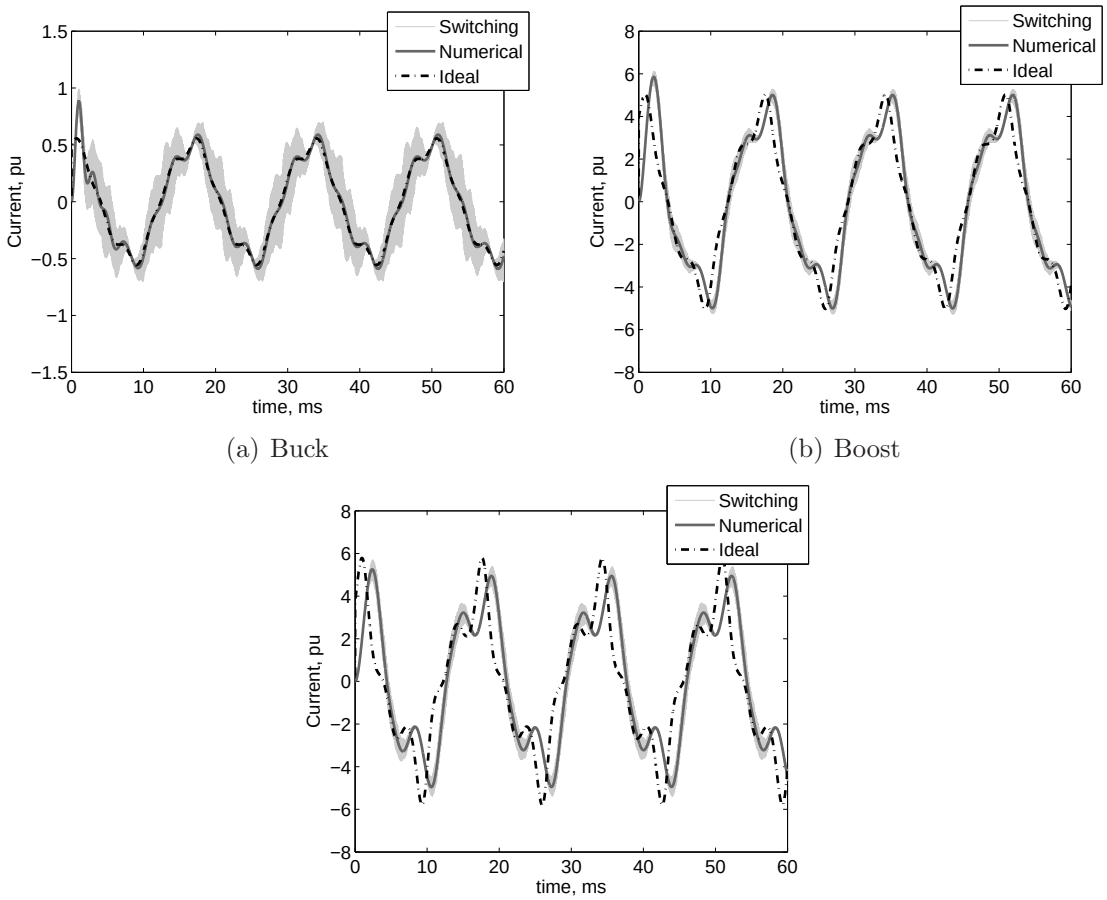
and for the buck-boost is,

$$d(t) = 0.6 + 0.05\sin(2\omega t) + 0.02\sin(4\omega t).$$

The results are per-unitized, where base current is the current injected by a fixed capacitor, $I_{base} = V_S\omega C$ and are given in Figure 4.2.

The plots validate that the numerical technique is adequately accurate. While the simplified analytical expressions are unable to fully model the dynamics introduced by R and L, they come very close to modeling the overall behavior of the topology. In fact, the simplified analytical expression is quite adequate in modeling most of the higher-order effects for the buck configuration. In contrast, the simplified expression for the boost expression is not as accurate, with the expression for buck-boost even less so. This is because in both the boost and buck-boost topologies, the inductor features much more prominently in the energy transfer between the main capacitor

and the source, and by eliminating it from the simplified expression, the voltage drop across the inductor is erroneously ignored.



(a) Buck

(b) Boost

(c) Buck-Boost

Figure 4.2: Comparison of the switching models, the numerically derived expressions, and the simplified analytical D-CAP inductor currents, with a 1 pu grid voltage for the three configurations with a non-constant duty cycle.

4.8 Operating Domain for VAR Compensation

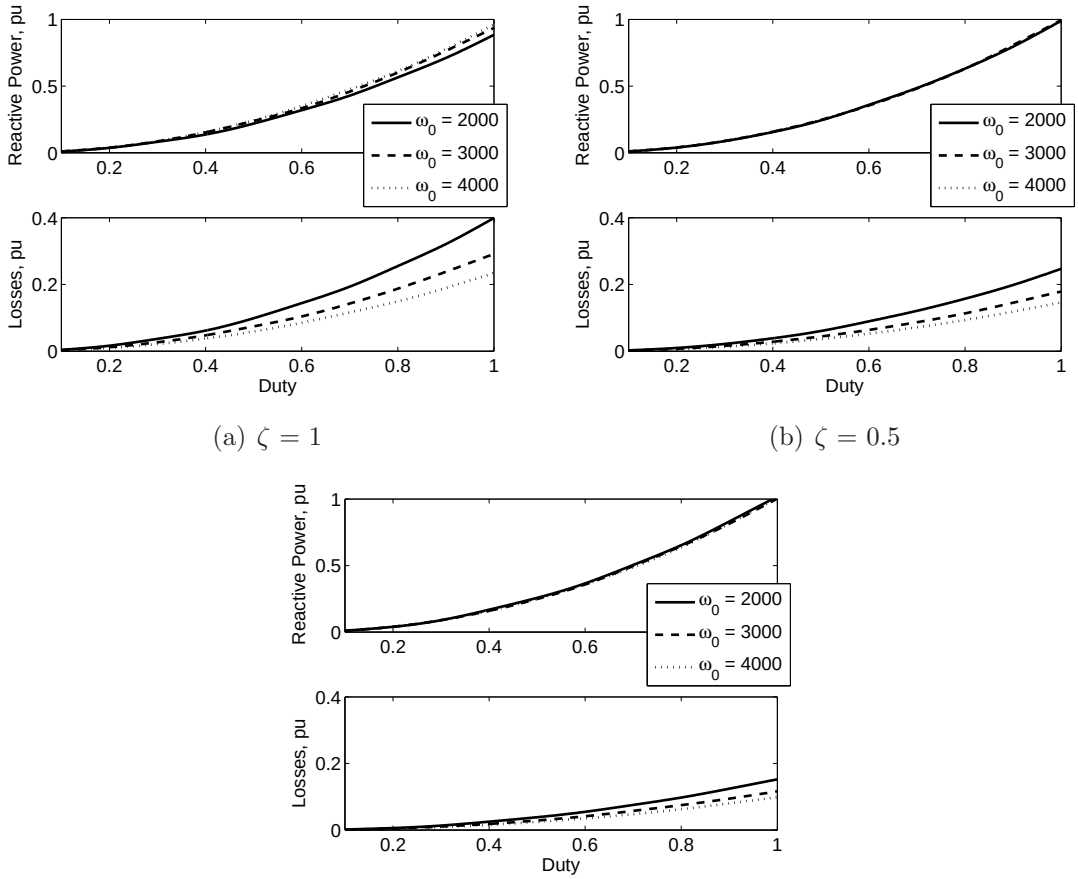
In Section 3.3.1, the operating domains of the three configurations of the D-CAP are described under idealized conditions. In actuality, the parasitics and filter component values make an impact in reducing those domains. The operating domains are re-evaluated in this section based on the analytical expressions derived in this chapter for operation under constant duty function, where the impact of the filter inductance

and parasitic losses have been accounted.

Figures 4.3-4.5 depict the plots of the operating domains with respect to the duty value, K_0, while Figures 4.6-4.8 plot the operating domains with respect to the line voltage, V_S, for the buck, the boost, and the buck-boost topologies. The operation domains are evaluated for different values of the natural frequency, ω_0, and damping factor, ζ. The reactive currents are per-unitized based on the fundamental current injected by a static capacitor with a capacitance of 1 mF and nominal grid voltage as calculated by, $I_{base} = V_S \omega C$. The losses are per-unitized based on the total power injected by the same static capacitor under nominal grid voltage, $Q_{base} = V_S^2 \omega C$. The natural frequencies and damping factors of each of the three topologies are defined in the previous section. For the boost and buck-boost case, their respective natural frequencies have been normalized by dividing by $(1 - K_0)$.

The first nine figures depict the operating domains as per-unitized reactive power and losses versus the duty cycle for a nominal 1 pu grid voltage.

The plots for the buck configuration in Figure 4.3 show that the impact of natural frequency and damping factor are minimal on the injected reactive current but make some impact on the losses, as is expected. The impact of natural frequency and damping factor are much more significant for the boost and buck-boost configurations as shown in Figures 4.4-4.5. The injected reactive power for these two configurations peak at a certain duty value before falling due to the losses and burgeoning dominance of the inductive elements at higher duty values. In fact, for both the boost and buck-boost configurations, the compensators start injecting lagging (inductive) VARs at higher duty values. This phenomenon is more pronounced for lower damping factors, and for lower natural frequencies for the boost and higher natural frequencies for the buck-boost. For applications that require lagging VARs, without resorting to using a D-IND, the D-CAP can be designed to provide a range of power from a small amount of lagging to relatively large amount of leading VARs.



(a) $\zeta = 1$

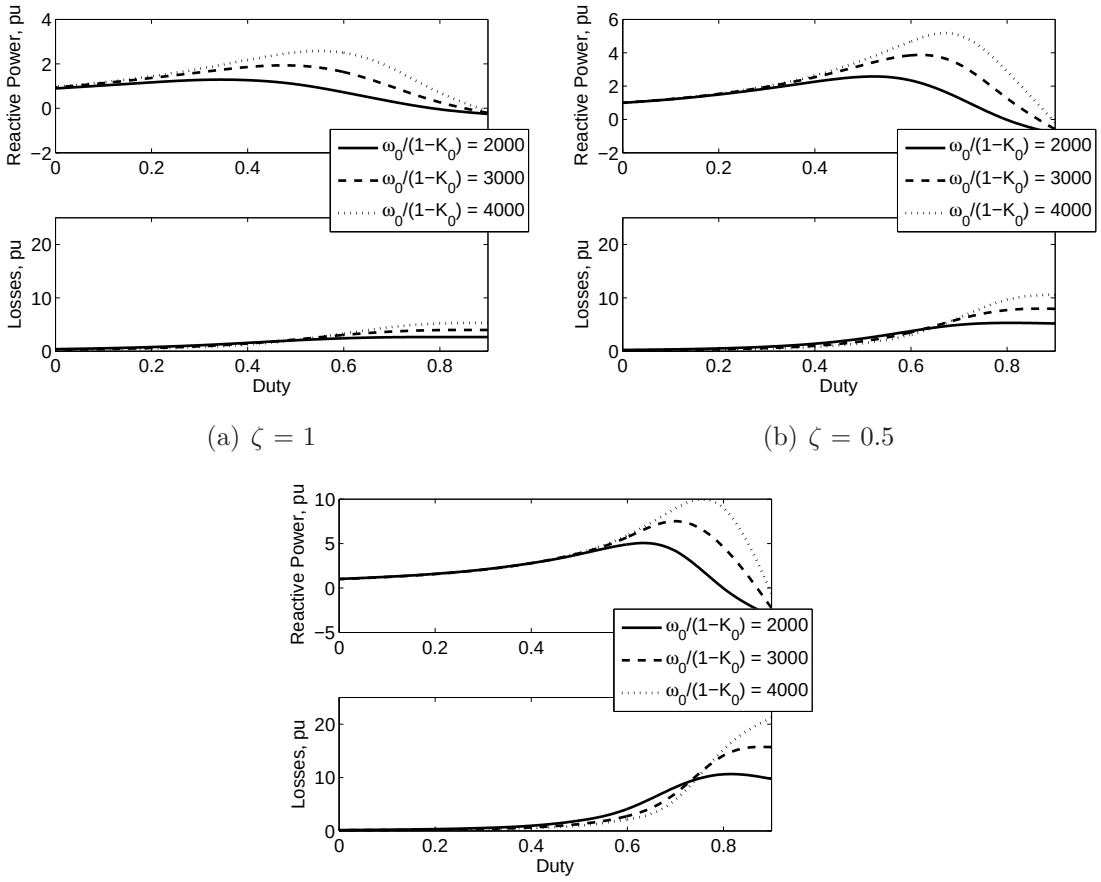
(b) $\zeta = 0.5$

(c) $\zeta = 0.25$

Figure 4.3: The operating regions of the buck D-CAP with respect to the duty function for different natural frequencies and damping factors for C = 1 mF.

The losses are seen to increase significantly with a higher natural frequency and lower damping factor.

The second set of nine figures depicts the operating domains as per-unitized reactive (leading) current and losses versus line voltage. The operating domains are limited to maintain the same losses as when the converters are operating under nominal grid conditions. The buck D-CAP results in Figure 4.6 show that the operating domains are very close to ideal where the maximum injection envelope is similar to the injection level of a static capacitor. Because the loss is highest under nominal grid condition, the loss minimization algorithm does not influence the operating domains.



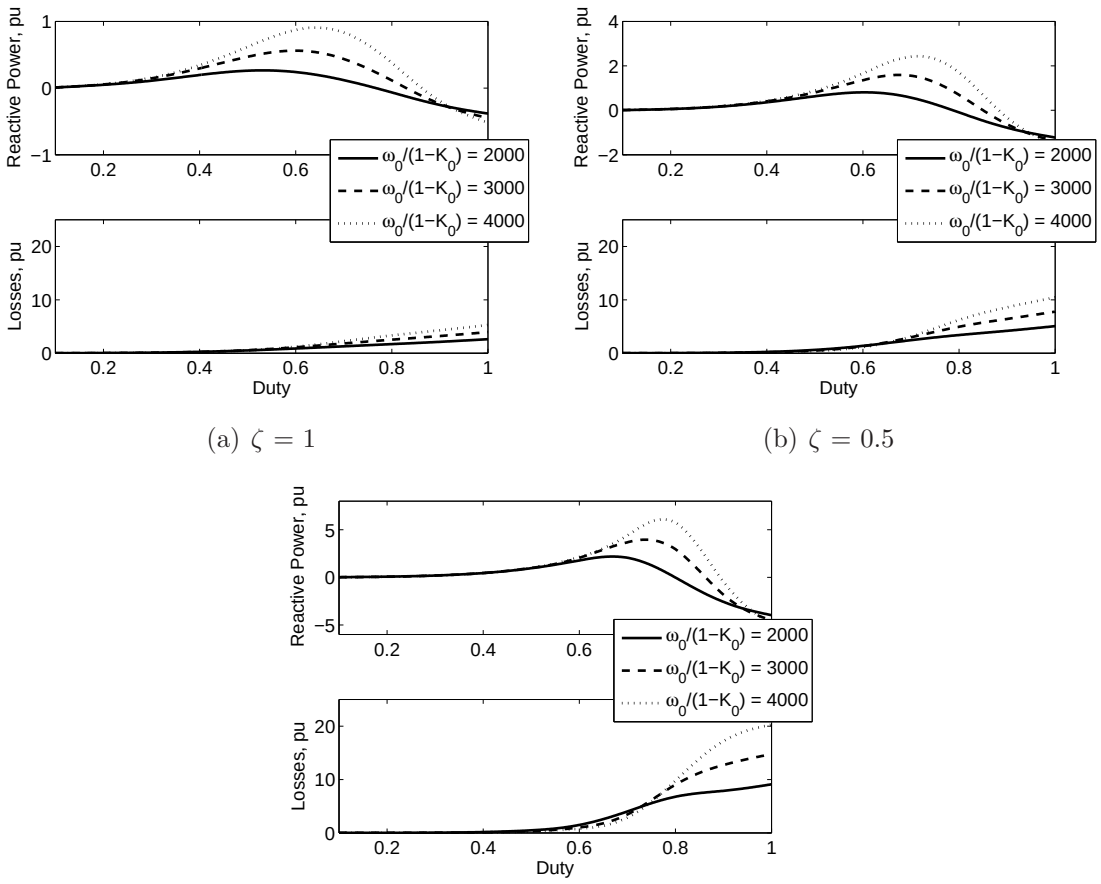
(a) $\zeta = 1$

(b) $\zeta = 0.5$

(c) $\zeta = 0.25$

Figure 4.4: The operating regions of the boost D-CAP with respect to the duty function for different natural frequencies and damping factors for C = 1 mF.

Both the boost and buck-boost operating domains are heavily limited by the maximum allowable losses, as observable by the flat tops of the loss curves in Figures 4.7 and 4.8. A designer may choose to allow losses to be in excess of the losses encountered under nominal grid conditions, which is a valid approach as the potential fault on the system only lasts for a limited period. This would have the effect of broadening the operating regions. However, this work takes a conservative stand where it is assumed that the voltage sag can last indefinitely and thus the performance is limited by the effectiveness of the thermal management system designed for nominal conditions. Both the boost and buck-boost topologies are also limited in their leading



(a) $\zeta = 1$

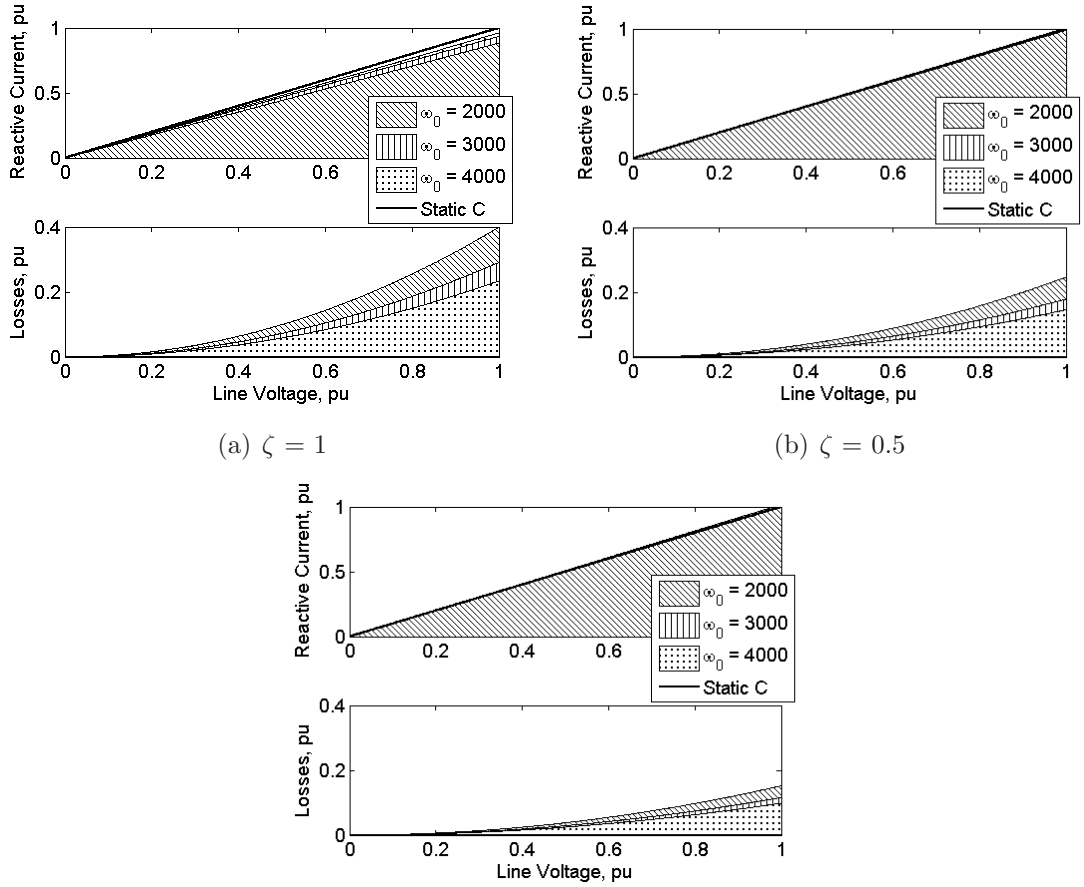
(b) $\zeta = 0.5$

(c) $\zeta = 0.25$

Figure 4.5: The operating regions of the buck-boost D-CAP with respect to the duty function for different natural frequencies and damping factors for C = 1 mF.

(capacitive) VAR injection capability by the filter inductance. Once a duty cycle exceeds certain level, depending on component and parasitic values, the topologies become not just more lossy but also more inductive.

It is clear from these figures that to maximize the operating region, the natural frequency needs to be high as possible, and the damping factor needs to be as low as possible. But the natural frequency needs to remain relatively low to suppress switching harmonics as well. Thus, trade-offs are required to optimize the overall performance.



(a) $\zeta = 1$

(b) $\zeta = 0.5$

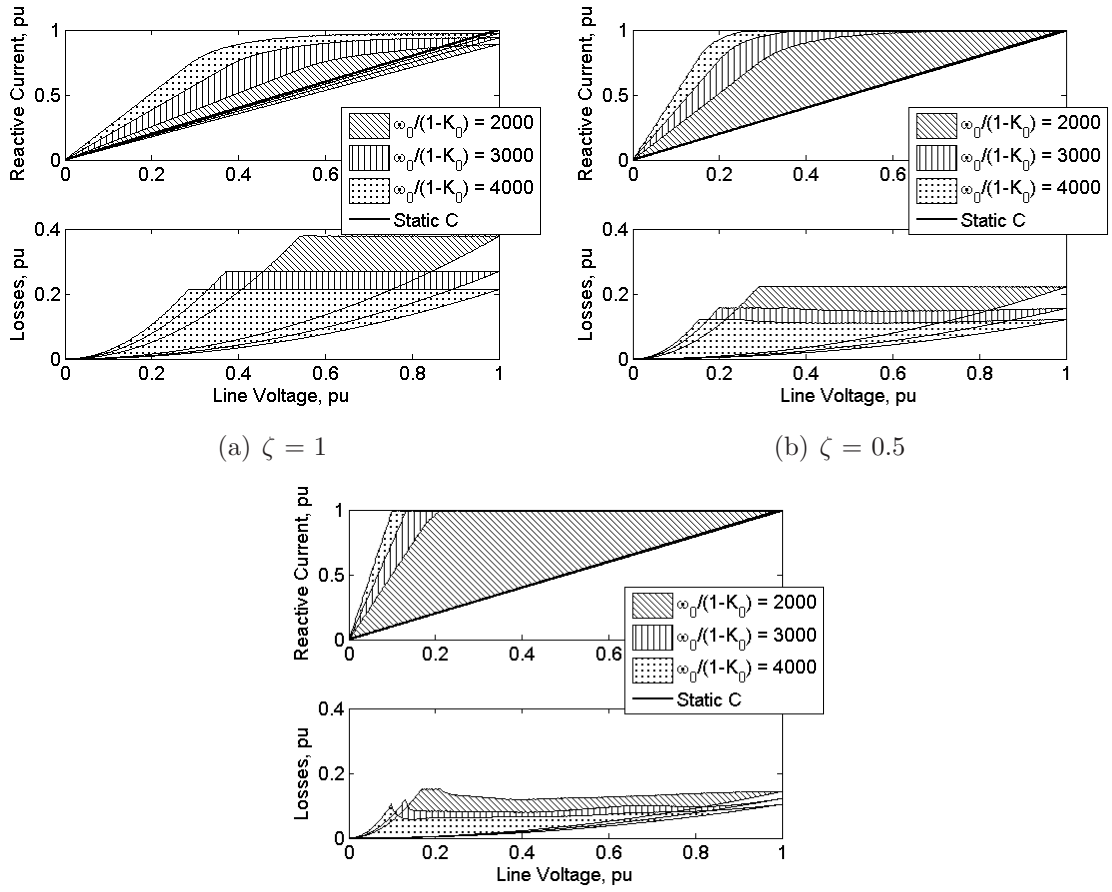
(c) $\zeta = 0.25$

Figure 4.6: The operating regions of the buck D-CAP with respect to the line voltage for different natural frequencies and damping factors for C = 1 mF.

4.9 Conclusions

Three sets of time-domain expressions describing the behavior of the buck, boost, and buck-boost D-CAP are presented in this chapter.

The first solution-set describes the operation of the converters under constant duty-cycle control, when the converter provides voltage support or power factor correction. The closed-form analytical expressions are able to model the parasitic losses as well as the impact of the filter inductance, both of which play a role in the converters' dynamic behavior. Based on these solutions, the operating domains are derived as a function of reactive current and losses versus duty cycle and line voltage. The



(a) $\zeta = 1$

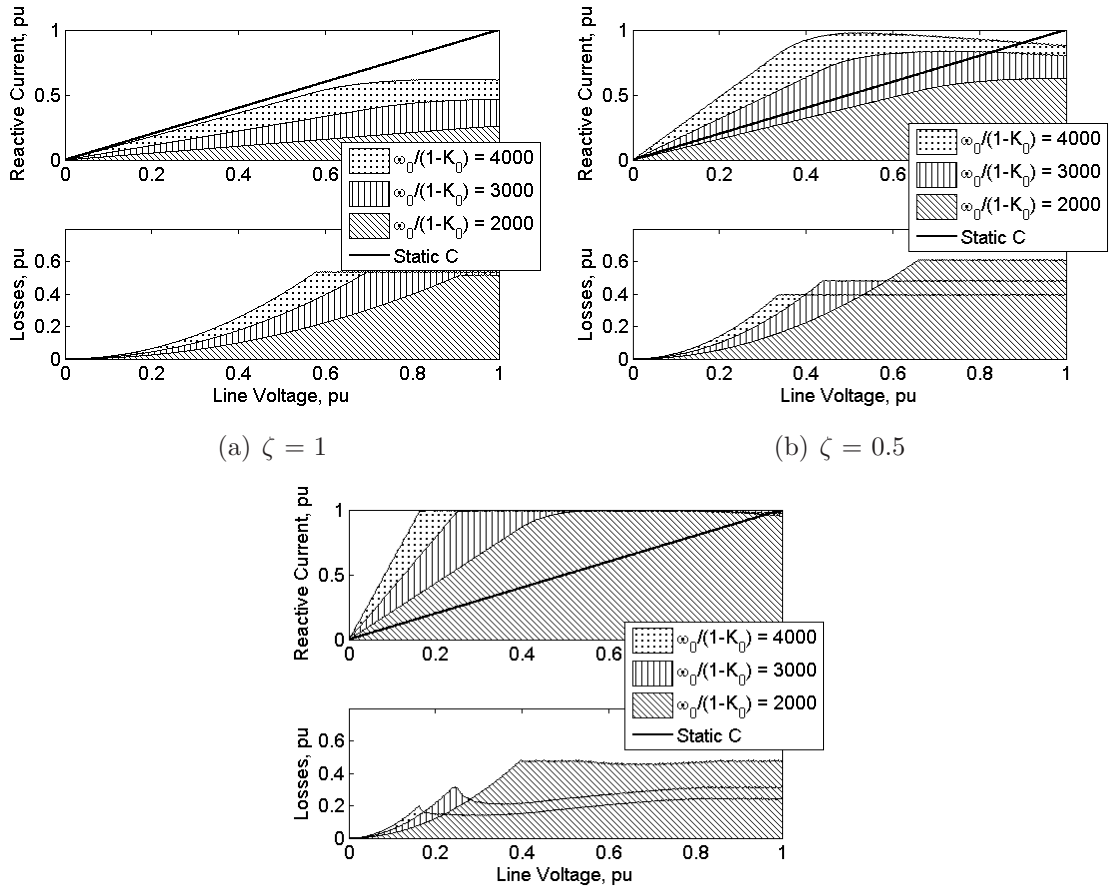
(b) $\zeta = 0.5$

(c) $\zeta = 0.25$

Figure 4.7: The operating regions of the boost D-CAP with respect to the line voltage for different natural frequencies and damping factors for C = 1 mF.

plots reveal that both the low natural frequency (large switching inductor) and high damping factor (high losses) of the converters can reduce the capability to supply reactive power.

The second solution-set describes the operation of the converter under EHM, when the converter provides both VAR and harmonic compensation. The governing equations under this operating condition are difficult to solve in the time domain. So, numerical expressions, through discretization of the time-based variables, are derived to model the behavior of the converters. Through comparisons with the switching models, the numerical expressions are found to be quite accurate in modeling the



(a) $\zeta = 1$

(b) $\zeta = 0.5$

(c) $\zeta = 0.25$

Figure 4.8: The operating regions of the buck-boost D-CAP with respect to the line voltage for different natural frequencies and damping factors for C = 1 mF.

transient and dynamic behavior of the converter.

The third and final solution set analytically describes the behavior of the converters under EHM. However, in solving the governing equations, the parasitic losses and the impact of filter inductors on sub-switching harmonics are assumed to be negligible. As long as these assumptions hold true, the solutions are adequately accurate. The simplified analytical expressions are critical in understanding the relationship between the modulation scheme and the generated harmonic currents used for active filtering. These expressions are used throughout this work to develop an understanding for the control and design of the DVHCs.

CHAPTER V

SMALL-SIGNAL MODELING

5.1 Introduction

The average and small-signal modeling efforts for the Dynamic VAR and Harmonic Compensators (DVHC) are driven by several key objectives:

1. To minimize the simulation time while capturing critical converter dynamics.
2. To study the response of the converters to various disturbances.
3. To understand dynamic interactions with the rest of the system, namely the power grid.
4. To understand the relationship between the control commands and corresponding response of the converters, so effective and robust controllers can be designed.

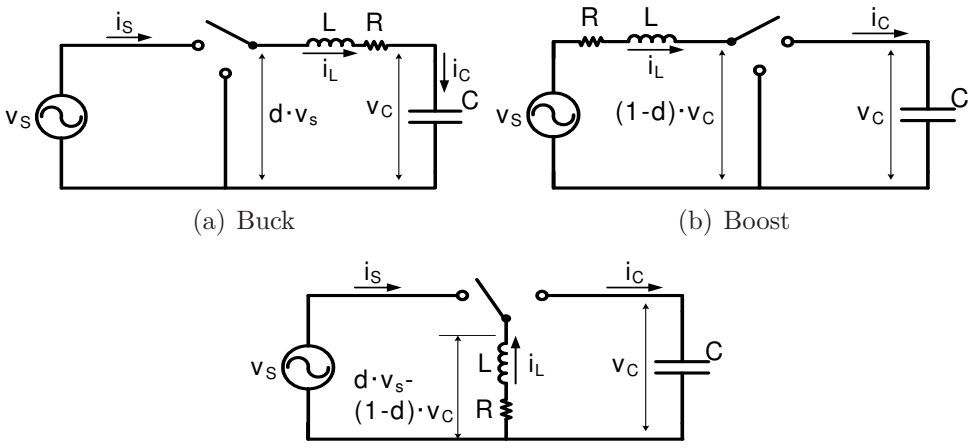
In this chapter large-signal (or average) models of the DHVC converters, in particular the Dynamic Capacitor (D-CAP), in both stationary (ABC) and synchronous (DQ0) reference frames are derived under the assumption of high-frequency synthesis, where the fast dynamics at and around the switching frequency are neglected. From the average DQ0 model of the plants, linear time-invariant (LTI) small-signal models of the D-CAP circuits are derived.

The small-signal models are derived in state-space representation, from which input-output transfer functions are extracted to study the frequency-response of the converters to various control and grid disturbances. The transfer functions, namely the ones relating the injected current to the duty function, are then used to model

the open-loop plant behavior. The transfer functions enable the design of effective linear controllers to dynamically regulate the VARs injected in a closed-loop manner.

5.2 Average Models in the Stationary Reference Frame

The first step in reduced-order modeling is to represent the converters functionally. To that end, the network of IGBT switches are represented with an ideal single-pole-double-throw (SPDT) switch, as depicted in Fig. 5.1, where rapid switching occurs between two positions.



(a) Buck (b) Boost

(c) Buck-Boost

Figure 5.1: The three configurations of the DACC drawn with a single-pole-double-throw switch.

The method of transforming the ideal switching model to an average one is a well known technique that has been used extensively for DC-DC converters [45]. The same approach is applied for the AC buck-, boost- and buck-boost-based converters in this work as well. The average model eliminates the higher-order effects induced by the relatively fast switching of the semiconductor devices. The key assumption here is that the maximum frequency of interest is significantly less than half the switching frequency, or $f_{h-max} << 1/2T_S$, per Nyquist's sampling theorem.

The switching function of the SPDT switch for the buck and boost topology is:

$$s(t) = \begin{cases} 1 & \text{for switch in position 1,} \\ 0 & \text{for switch in position 2.} \end{cases} \tag{5.1}$$

The switching function for the buck-boost cannot be expressed as simply, but the same concept applies: the switching states are finite and discrete. For the buck-boost, when the switch is in one position, grid voltage is applied across the filter inductor, and when the switch is in the other position, the capacitor voltage is applied across the filter inductor, or $V_L = s(t) V_S + \bar{s}(t) V_C$, where $\bar{s}(t)$ is complementary of the switch function $s(t)$.

The averaging operator used in obtaining the average model is:

$$\langle x(t) \rangle_{T_S} \equiv \overline{x}(t) \equiv \frac{1}{T_S} \int_{t-T_S}^{t} x(\tau)\, d\tau, \tag{5.2}$$

where the period, T_S, is the window over which the averaging takes place. Applying the averaging operator to a sum of arbitrary functions and to derivative of some arbitrary function, if the function is differentiable and integrable, the following two properties are observed:

$$\overline{\alpha x(t) + \beta y(t)} = \frac{1}{T_S} \int_{t-T_S}^{t} [\alpha x(\tau) + \beta y(\tau)]\, d\tau = \alpha \overline{x(t)} + \beta \overline{y(t)},$$

$$\overline{\frac{dx(t)}{dt}} = \frac{1}{T_S} \int_{t-T_S}^{t} \left[\frac{dx(\tau)}{d\tau}\right] d\tau \approx \frac{d}{dt}\left[\frac{1}{T_S} \int_{t-T_S}^{t} x(\tau)\, d\tau\right] = \frac{d\overline{x}}{dt}.$$

Application of the averaging operator to the switching function, $s(t)$, over the switching period results in the duty-cycle function:

$$d(t) \equiv \overline{s(t)} = \frac{1}{T_S} \int_{t-T_S}^{t} s(\tau)\, d\tau$$

This is the same duty function that the previous chapters have employed under the assumption of high-frequency synthesis. Applying the averaging operator to the circuits of Figure 5.1, the following set of state equations for each of the three D-CAP configurations result:

Buck:

$$L\frac{d\bar{i}_L}{dt} = d(t)\,\overline{v}_S - \overline{v}_C - R\bar{i}_L \tag{5.3}$$

$$C\frac{d\overline{v}_C}{dt} = \bar{i}_L \tag{5.4}$$

Boost:

$$L\frac{d\bar{i}_L}{dt} = \overline{v}_S - (1-d(t))\,\overline{v}_C - R\bar{i}_L \tag{5.5}$$

$$C\frac{d\overline{v}_C}{dt} = (1-d(t))\,\bar{i}_L \tag{5.6}$$

Buck-Boost:

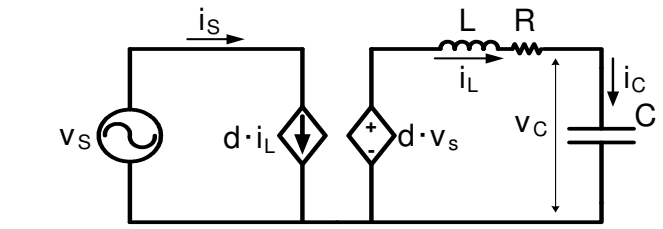
$$L\frac{d\bar{i}_L}{dt} = d(t)\,\overline{v}_S - (1-d(t))\,\overline{v}_C - R\bar{i}_L \tag{5.7}$$

$$C\frac{d\overline{v}_C}{dt} = (1-d(t))\,\bar{i}_L \tag{5.8}$$

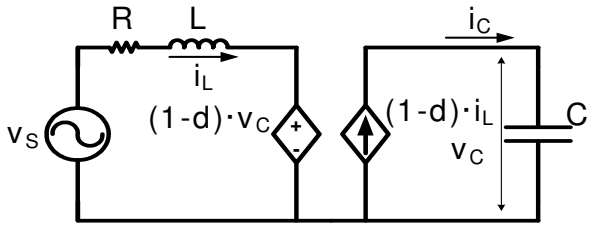
Expressing these averaged expressions as circuit diagrams, Figure 5.2 depicts the average models. In comparing the average with the switching models, the average models are found to be quite accurate in modeling the low-order dynamics of the system. An example comparison is shown in Figure 5.3 for the operating conditions and component values summarized by Table 5.1.

Table 5.1: The operating conditions and component values used in comparison of the average and the switching models.

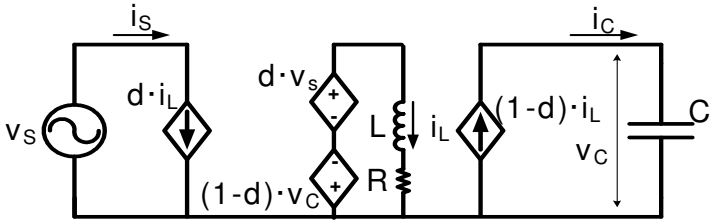
Operating Condition / Component	Value		Description
V_S	480	V	Line-to-line voltage
C	1	mF	Main capacitor
L	100	μH	Switching inductor
R	0.1	Ω	Equivalent parasitic resistance
D	0.5	-	Buck duty
	0.2	-	Boost duty
	0.4	-	Buck-boost duty



(a) Buck



(b) Boost



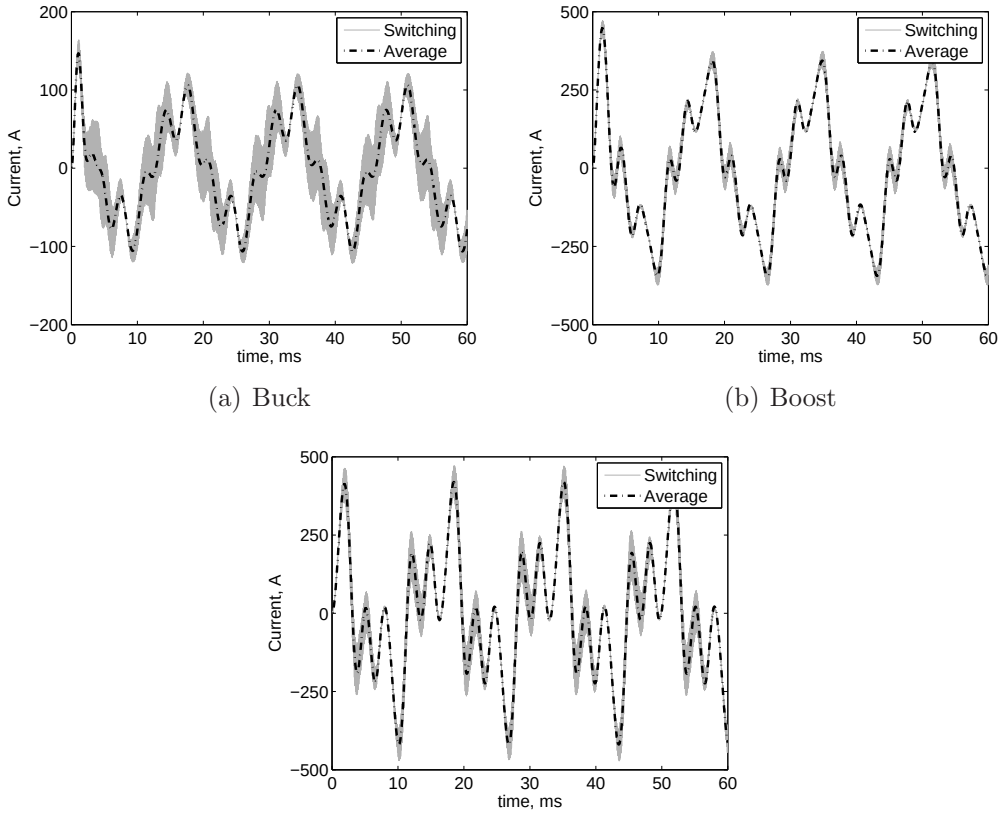
(c) Buck-Boost

Figure 5.2: The average models of the three D-CAP configurations.

5.3 Three-Phase Large-Signal Model

While the average models eliminate high-order effects attributed to the switching of the semiconductor devices, the models remain largely non-linear. In order to design with linear controllers, linear time-invariant (LTI) small-signal plant models are needed. The D-CAP topologies are direct AC converters with sinusoidal signals. Deriving time-invariant models requires coordinate transformation where vectors that are rotating are mapped to a coordinate reference frame where the same vectors are stationary.

One such a coordinate transformation, Park's transformation, initially developed for electrical machines, has been used extensively in the field of power electronics to model inverters and rectifiers. The transformation maps vectors from the stationary



(a) Buck

(b) Boost

(c) Buck-Boost

Figure 5.3: The comparisons of the switching and the large-signal (average) models of the three D-CAP configurations.

reference frame, $\vec{X}_{abc}$, to the synchronous reference frame, $\vec{X}_{dq0}$, where the sinusoidal ABC terms are mapped as constant DQ0 terms. In the synchronous reference frame, all the state-of-the-art control and modeling techniques developed for DC-DC power converters are directly applicable. To enable the transformation, the D-CAP circuits are analyzed as a three-phase system.

While the D-CAP is a three-phase system, it is implemented as single-phase units, therefore each phase is controlled independently of the other two phases. This allows the D-CAP to source unbalanced reactive power, a key feature that separates the D-CAP systems from the state-of-the-art three-phase voltage-source-inverter-based systems. In obtaining the three-phase average models of the D-CAP circuits, the

other two phases can be considered to be "virtual", serving only to enable coordinate transformation to a domain where all the vectors are DC or constant.

Alternatively, the three phases can be actual units as well but with each of the three phases controlled using the same duty command. For such a system, the model derived with the two virtual phases remains applicable.

A single-phase converter can also be modeled as a two-phase system in the stationary reference frame where the second phase is considered to be a virtual circuit that is orthogonal (offset by 90 degrees) to the primary phase. This two-dimensional model can be mapped to the synchronous reference frame where the two vectors are stationary. However, as part of this work, to generalize the approach of converting the plant models from stationary to synchronous reference frame, three-phase transformation is demonstrated.

The three-phase average models of the D-CAP circuits are expressed in the stationary reference frame as follows:

Three-phase buck:

$$\frac{d}{dt}\bar{i}_{Labc} = \frac{1}{L}d_{abc}\overline{v}_{Sabc} - \frac{R}{L}\bar{i}_{Labc} - \frac{1}{L}\overline{v}_{Cabc} \tag{5.9}$$

$$\frac{d}{dt}\overline{v}_{Cabc} = \frac{1}{C}\bar{i}_{Labc} \tag{5.10}$$

$$\bar{i}_{Sabc} = d_{abc}\bar{i}_{Labc} \tag{5.11}$$

Three-phase boost:

$$\frac{d}{dt}\bar{i}_{Labc} = \frac{1}{L}\overline{v}_{Sabc} - \frac{R}{L}\bar{i}_{Labc} - \frac{1}{L}\left(\mathrm{I} - d_{abc}\right)\overline{v}_{Cabc} \tag{5.12}$$

$$\frac{d}{dt}\overline{v}_{Cabc} = \frac{1}{C}\left(\mathrm{I} - d_{abc}\right)\bar{i}_{Labc} \tag{5.13}$$

$$\bar{i}_{Sabc} = \bar{i}_{Labc} \tag{5.14}$$

Three-phase buck-boost:

$$\frac{d}{dt}\bar{i}_{Labc} = \frac{1}{L}d_{abc}\overline{v}_{Sabc} - \frac{R}{L}\bar{i}_{Labc} - \frac{1}{L}\left(\mathrm{I} - d_{abc}\right)\overline{v}_{Cabc} \tag{5.15}$$

$$\frac{d}{dt}\overline{v}_{Cabc} = \frac{1}{C}\left(\mathrm{I} - d_{abc}\right)\bar{i}_{Labc} \tag{5.16}$$

$$\bar{i}_{Sabc} = d_{abc}\bar{i}_{Labc} \tag{5.17}$$

where

$$d_{abc} = \begin{bmatrix} d_a & 0 & 0 \\ 0 & d_b & 0 \\ 0 & 0 & d_c \end{bmatrix} \equiv \text{duty function matrix},$$

$$\bar{i}_{Labc} = \begin{bmatrix} \bar{i}_{La} & \bar{i}_{Lb} & \bar{i}_{Lc} \end{bmatrix}^T \equiv \text{inductor current vector},$$

$$\bar{i}_{Sabc} = \begin{bmatrix} \bar{i}_{Sa} & \bar{i}_{Sb} & \bar{i}_{Sc} \end{bmatrix}^T \equiv \text{D-CAP injected current vector},$$

$$\overline{v}_{Cabc} = \begin{bmatrix} \overline{v}_{Ca} & \overline{v}_{Cb} & \overline{v}_{Cc} \end{bmatrix}^T \equiv \text{main capacitor voltage vector},$$

$$\overline{v}_{Sabc} = \begin{bmatrix} \overline{v}_{Sa} & \overline{v}_{Sb} & \overline{v}_{Sc} \end{bmatrix}^T \equiv \text{line voltage vector}.$$

ABC-to-DQ0 transformation is employed in mapping the vectors from the stationary to synchronous (rotating) reference frame, which is defined by the following transformation matrix for a three-phase system:

$$T_{dq0/abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\omega t) & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) \\ \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{5.18}$$

In this derivation, $d_a = d_b = d_c = k_0$. This implies that all three phases are controlled using a single, constant duty cycle. As the DVHC converters are controlled on a single-phase basis, and with the other two phases considered to be "virtual" circuits leveraged to derive the DQ0 components, the assumption that the duty cycle is the same for all three-phases is valid.

Further, this assumption implies that the even harmonic terms are also not considered in the duty-cycle function. The harmonics are not considered because the ABC-to-DQ0 transformation maps stationary reference frame vectors to synchronous reference frame revolving at a single frequency, such that when the harmonic terms are mapped over, they remain sinusoidal; the harmonics are simply shifted down by the frequency of the synchronous reference frame. The presence of the steady-state sinusoidal terms prevents the development of a time-invariant model, making it difficult to derive the necessary transfer functions.

5.3.1 Buck D-CAP

In applying the property, $\vec{X}_{abc} = T^{-1}_{dq0/abc} \cdot \vec{X}_{dq0}$, to the ABC model, the following intermediate expressions result:

$$\frac{d}{dt}\left(T^{-1}\bar{i}_{Ldq0}\right) = \frac{1}{L}k_0 T^{-1}\overline{v}_{Sdq0} - \frac{R}{L}T^{-1}\bar{i}_{Ldq0} - \frac{1}{L}T^{-1}\overline{v}_{Cdq0} \tag{5.19}$$

$$\frac{d}{dt}\left(T^{-1}\overline{v}_{Cdq0}\right) = \frac{1}{C}T^{-1}\bar{i}_{Ldq0} \tag{5.20}$$

$$T^{-1}\bar{i}_{Sdq0} = k_0 T^{-1}\bar{i}_{Ldq0} \tag{5.21}$$

Multiplying through by T and applying the properties,

$$\frac{d}{dt}\left(T^{-1}_{dq0/abc} \cdot \vec{X}_{dq0}\right) = \frac{d}{dt}\left(T^{-1}_{dq0/abc}\right) \cdot \vec{X}_{dq0} + T^{-1}_{dq0/abc} \cdot \frac{d}{dt}\vec{X}_{dq0}, \tag{5.22}$$

and

$$T_{dq0/abc}\frac{dT^{-1}_{dq0/abc}}{dt} = \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \tag{5.23}$$

where ω is the frequency of the synchronous reference frame, and rearranging the terms result in the average DQ0 model of the buck D-CAP given as:

$$\frac{d}{dt}\bar{i}_{Ldq0} = \frac{1}{L}k_0\overline{v}_{Sdq0} - \begin{bmatrix} \frac{R}{L} & -\omega & 0 \\ \omega & \frac{R}{L} & 0 \\ 0 & 0 & \frac{R}{L} \end{bmatrix} \bar{i}_{Ldq0} - \frac{1}{L}\overline{v}_{Cdq0} \tag{5.24}$$

$$\frac{d}{dt}\overline{v}_{Cdq0} = \frac{1}{C}\bar{i}_{Ldq0} - \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \overline{v}_{Cdq0} \tag{5.25}$$

$$\bar{i}_{Sdq0} = k_0\bar{i}_{Ldq0} \tag{5.26}$$

The equivalent circuit diagrams are given by Figure 5.4.

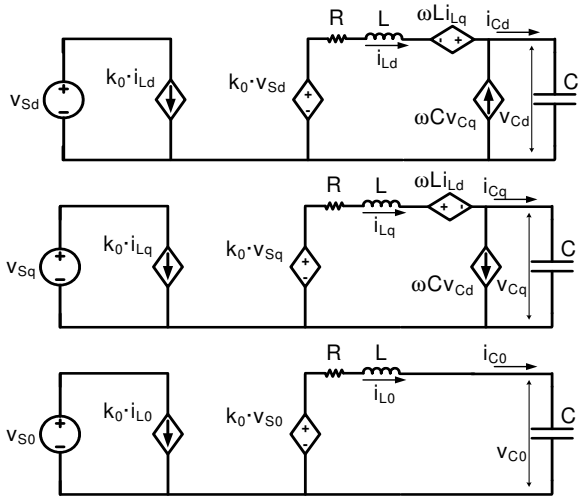


Figure 5.4: The average DQ0 model of the buck D-CAP.

5.3.2 Boost D-CAP

Following the same approach, the average DQ0 model of the boost D-CAP is derived as:

$$\frac{d}{dt}\bar{i}_{Ldq0} = \frac{1}{L}\overline{v}_{Sdq0} - \begin{bmatrix} \frac{R}{L} & -\omega & 0 \\ \omega & \frac{R}{L} & 0 \\ 0 & 0 & \frac{R}{L} \end{bmatrix} \bar{i}_{Ldq0} - (1-k_0)\frac{1}{L}\overline{v}_{Cdq0} \tag{5.27}$$

$$\frac{d}{dt}\overline{v}_{Cdq0} = (1-k_0)\frac{1}{C}\overline{i}_{Ldq0} - \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \overline{v}_{Cdq0} \tag{5.28}$$

$$\overline{i}_{Sdq0} = \overline{i}_{Ldq0} \tag{5.29}$$

The equivalent circuit diagrams are given by Figure 5.5.

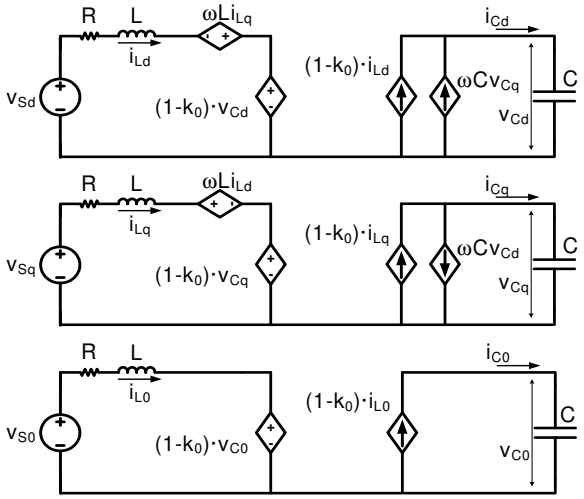


Figure 5.5: The average DQ0 model of the boost D-CAP.

5.3.3 Buck-Boost D-CAP

Applying the same approach as the other two topologies to the buck-boost D-CAP, the transformation of the average model from the stationary to the synchronous reference frame results in:

$$\frac{d}{dt}\overline{i}_{Ldq0} = \frac{1}{L}k_0\overline{v}_{Sdq0} - \begin{bmatrix} \frac{R}{L} & -\omega & 0 \\ \omega & \frac{R}{L} & 0 \\ 0 & 0 & \frac{R}{L} \end{bmatrix} \overline{i}_{Ldq0} - \frac{1}{L}(1-k_0)\,\overline{v}_{Cdq0} \tag{5.30}$$

$$\frac{d}{dt}\overline{v}_{Cdq0} = \frac{1}{C}(1-k_0)\,\overline{i}_{Ldq0} - \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \overline{v}_{Cdq0} \tag{5.31}$$

$$\bar{i}_{Sdq0} = k_0 \bar{i}_{Ldq0} \tag{5.32}$$

The equivalent circuit diagrams are then given by Figure 5.6.

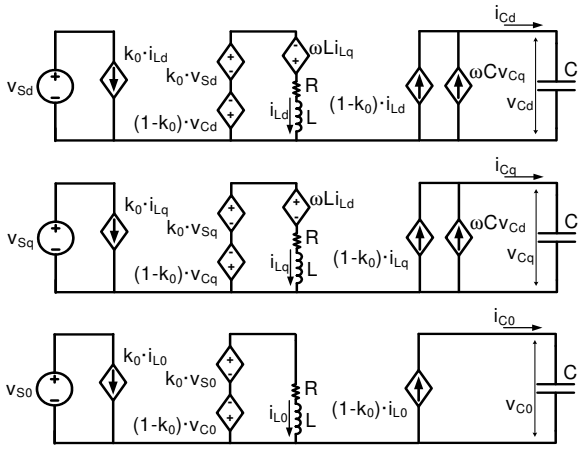


Figure 5.6: The average DQ0 model of the buck-boost D-CAP.

The resulting average models in the synchronous reference frame, while time-invariant, are still non-linear.

5.4 Approach to Linearization

An autonomous dynamic system given by:

$$\frac{d\vec{x}}{dt} = \vec{f}(\vec{x}, \vec{u})$$

is linearizable if it can be resolved into the form:

$$\frac{d\vec{x}}{dt} = \mathbf{A}\vec{x} + \mathbf{B}\vec{u}$$

Taylor series is used to represent the system, $\vec{f}(\vec{x}, \vec{u})$. The system dynamics are approximated by taking the first few terms and neglecting the higher order terms as their impact is assumed to be negligible. The resulting approximation is still not linear. To linearize it, the system is perturbed around an equilibrium point $\left(\vec{X}, \vec{U}\right)$.

If the function $\vec{f}$ is analytic, the function can be represented using the Taylor series:

$$\begin{aligned}\vec{f}(\vec{x},\vec{u}) = \vec{f}(\vec{x}_0,\vec{u}_0) &+ \frac{\partial \vec{f}(\vec{x}_0,\vec{u}_0)}{\partial \vec{x}} \cdot (\vec{x}-\vec{x}_0) + \frac{\partial \vec{f}(\vec{x}_0,\vec{u}_0)}{\partial \vec{u}} \cdot (\vec{u}-\vec{u}_0) \\ &+ \frac{1}{2!}\left[\frac{\partial^2 \vec{f}(\vec{x}_0,\vec{u}_0)}{\partial \vec{x}^2} \cdot (\vec{x}-\vec{x}_0)^2 + \frac{\partial^2 \vec{f}(\vec{x}_0,\vec{u}_0)}{\partial \vec{x}\partial \vec{u}} \cdot (\vec{x}-\vec{x}_0)(\vec{u}-\vec{u}_0)\right. \\ &\left. + \frac{\partial^2 \vec{f}(\vec{x}_0,\vec{u}_0)}{\partial \vec{u}^2} \cdot (\vec{u}-\vec{u}_0)^2\right] + \cdots\end{aligned}$$

The first three terms in the Taylor series is retained as an approximation of $\vec{f}$:

$$\vec{f}(\vec{x},\vec{u}) = \vec{f}(\vec{x}_0,\vec{u}_0) + \frac{\partial \vec{f}(\vec{x}_0,\vec{u}_0)}{\partial \vec{x}} \cdot (\vec{x}-\vec{x}_0) + \frac{\partial \vec{f}(\vec{x}_0,\vec{u}_0)}{\partial \vec{u}} \cdot (\vec{u}-\vec{u}_0) \tag{5.33}$$

The expression is rewritten as follows:

$$\begin{aligned}\underbrace{\vec{f}(\vec{x},\vec{u})}_{\dot{\vec{x}}} = &\underbrace{\frac{\partial \vec{f}(\vec{x}_0,\vec{u}_0)}{\partial \vec{x}}}_{\mathbf{A}} \cdot \vec{x} + \underbrace{\frac{\partial \vec{f}(\vec{x}_0,\vec{u}_0)}{\partial \vec{u}}}_{\mathbf{B}} \cdot \vec{u} \\ &+ \underbrace{\vec{f}(\vec{x}_0,\vec{u}_0) - \frac{\partial \vec{f}(\vec{x}_0,\vec{u}_0)}{\partial \vec{x}} \cdot \vec{x}_0 - \frac{\partial \vec{f}(\vec{x}_0,\vec{u}_0)}{\partial \vec{u}} \cdot \vec{u}_0}_{\overline{\overline{\neq 0}}}\end{aligned} \tag{5.34}$$

The system is still non-linear due to the presence of the last term; it does not equal to zero. If $(\vec{x}_0,\vec{u}_0)$ is an equilibrium point $\left(\vec{X},\vec{U}\right)$, and $\left(\tilde{\vec{x}},\tilde{\vec{u}}\right)$ is perturbation around this equilibrium point, such that,

$$\vec{x} = \vec{X} + \tilde{\vec{x}}, \tag{5.35}$$

$$\vec{u} = \vec{U} + \tilde{\vec{u}}. \tag{5.36}$$

Then it follows that,

$$\vec{f}\left(\vec{X},\vec{U}\right) \equiv 0, \tag{5.37}$$

$$\frac{d\vec{X}}{dt} = 0, \tag{5.38}$$

and,

$$\frac{d\vec{x}}{dt} = \frac{d\vec{X}}{dt} + \frac{d\tilde{\vec{x}}}{dt} = \frac{d\tilde{\vec{x}}}{dt}. \tag{5.39}$$

The final linearized model of the dynamic system is then given by,

$$\frac{d\tilde{\vec{x}}}{dt} = \mathbf{A}\tilde{\vec{x}} + \mathbf{B}\tilde{\vec{u}}, \tag{5.40}$$

where

$$\mathbf{A} = \frac{\partial \vec{f}\,(\vec{x},\vec{u})}{\partial \vec{x}}\,|_{(\vec{X},\vec{U})},$$
$$\mathbf{B} = \frac{\partial \vec{f}\,(\vec{x},\vec{u})}{\partial \vec{u}}|_{(\vec{X},\vec{U})}.$$

5.5 Linear Time-Invariant Small-Signal Model

In summary, an arbitrary non-linear product, $\overline{u}\cdot\overline{v}$, linearized around quiescent points, U and V, is expressed as $U\tilde{v}+V\tilde{u}$, where $\tilde{v}$ and $\tilde{u}$ are small-signal perturbation around the quiescent points. The same approach is applied to the average (large-signal) DQ0 models of the buck, boost, and buck-boost D-CAP to derive the linear small-signal models.

5.5.1 Buck D-CAP

The small-signal model of the buck D-CAP is given by,

$$\frac{d}{dt}\tilde{i}_{Ldq0} = \frac{1}{L}V_{Sdq0}\tilde{k}_0 + \frac{1}{L}K_0\tilde{v}_{Sdq0} - \begin{bmatrix} \frac{R}{L} & -\omega & 0 \\ \omega & \frac{R}{L} & 0 \\ 0 & 0 & \frac{R}{L} \end{bmatrix}\tilde{i}_{Ldq0} - \frac{1}{L}\tilde{v}_{Cdq0}, \tag{5.41}$$

$$\frac{d}{dt}\tilde{v}_{Cdq0} = \frac{1}{C}\tilde{i}_{Ldq0} - \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\tilde{v}_{Cdq0}, \tag{5.42}$$

$$\tilde{i}_{Sdq0} = I_{Ldq0}\tilde{k}_0 + K_0\tilde{i}_{Ldq0}. \tag{5.43}$$

For the input, output and state definitions given by,

$$\tilde{\vec{x}} = \begin{bmatrix} \tilde{i}_{Ld} & \tilde{i}_{Lq} & \tilde{i}_{L0} & \tilde{v}_{Cd} & \tilde{v}_{Cq} & \tilde{v}_{C0} \end{bmatrix}^T,$$

$$\tilde{\vec{u}} = \tilde{k}_0,$$

$$\tilde{\vec{v}} = \begin{bmatrix} \tilde{v}_{Sd} & \tilde{v}_{Sq} & \tilde{v}_{S0} \end{bmatrix}^T,$$

$$\tilde{\vec{y}} = \begin{bmatrix} \tilde{i}_{Sd} & \tilde{i}_{Sq} & \tilde{i}_{S0} \end{bmatrix}^T,$$

the state-space representation is derived as:

$$\begin{aligned} \frac{d\tilde{\vec{x}}}{dt} = & \underbrace{\begin{bmatrix} -R/L & \omega & 0 & -1/L & 0 & 0 \\ -\omega & -R/L & 0 & 0 & -1/L & 0 \\ 0 & 0 & -R/L & 0 & 0 & 1/L \\ 1/C & 0 & 0 & 0 & \omega & 0 \\ 0 & 1/C & 0 & -\omega & 0 & 0 \\ 0 & 0 & 1/C & 0 & 0 & 0 \end{bmatrix}}_{\mathbf{A}} \tilde{\vec{x}} \\ & + \underbrace{\begin{bmatrix} V_{Sd}/L \\ V_{Sq}/L \\ V_{S0}/L \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{B}} \tilde{\vec{u}} + \underbrace{\begin{bmatrix} K_0/L & 0 & 0 \\ 0 & K_0/L & 0 \\ 0 & 0 & K_0/L \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}}_{\mathbf{E}} \tilde{\vec{v}}, \end{aligned} \tag{5.44}$$

$$\tilde{\vec{y}} = \underbrace{\begin{bmatrix} K_0 & 0 & 0 & 0 & 0 & 0 \\ 0 & K_0 & 0 & 0 & 0 & 0 \\ 0 & 0 & K_0 & 0 & 0 & 0 \end{bmatrix}}_{\mathbf{C}} \tilde{\vec{x}} + \underbrace{\begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{L0} \end{bmatrix}}_{\mathbf{D}} \tilde{\vec{u}}, \tag{5.45}$$

In determining the DC quantities in equilibrium, namely the state vectors $\vec{I}_{Ldq0}$ and $\vec{V}_{Cdq0}$, the large-signal average model given by Equations (5.24)-(5.26) is considered.

Letting the average terms be DC, the differential terms converge to zero with respect to time: $\dot{I}_{Ldq0} = \dot{V}_{Cdq0} = 0$. With the constant duty-cycle term, K_0, set to the desired value and the input DC voltage vector, $\vec{V}_{Sdq0}$, known, the DC state vectors are found:

$$\begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{L0} \end{bmatrix} = \begin{bmatrix} \left(K_0\omega C\left(\omega^2 LCV_{Sq} + \omega RCV_{Sd} - V_{Sq}\right)\right)/\Psi \\ \left(K_0\omega C\left(\omega^2 LCV_{Sd} + \omega RCV_{Sq} - V_{Sd}\right)\right)/\Psi \\ 0 \end{bmatrix}, \tag{5.46}$$

$$\begin{bmatrix} V_{Cd} \\ V_{Cq} \\ V_{C0} \end{bmatrix} = \begin{bmatrix} \left(K_0\left(V_{Sd} + \omega RCV_{Sq} - \omega^2 LCV_{Sd}\right)\right)/\Psi \\ \left(K_0\left(V_{Sq} - \omega RCV_{Sd} - \omega^2 LCV_{Sq}\right)\right)/\Psi \\ K_0 V_{S0} \end{bmatrix}, \tag{5.47}$$

where

$$\Psi = \omega^4 L^2C^2 + \omega^2 R^2C^2 - 2\omega^2 LC + 1.$$

Converting the state-space model into an equivalent circuit model, the DQ0 small-signal model of the buck D-CAP is given by Figure 5.7.

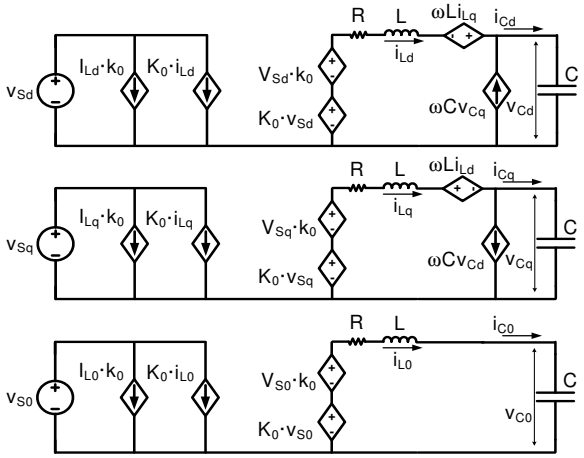


Figure 5.7: The linear small-signal DQ0 model of the buck D-CAP.

5.5.2 Boost D-CAP

The average DQ0 model of the boost is linearized using the same approach. The resulting small-signal model expressed using state-space representation is given by,

$$\frac{d\tilde{\vec{x}}}{dt} = \underbrace{\begin{bmatrix} -R/L & \omega & 0 & -K_0^P/L & 0 & 0 \\ -\omega & -R/L & 0 & 0 & -K_0^P/L & 0 \\ 0 & 0 & -R/L & 0 & 0 & -K_0^P/L \\ K_0^P/C & 0 & 0 & 0 & \omega & 0 \\ 0 & K_0^P/C & 0 & -\omega & 0 & 0 \\ 0 & 0 & K_0^P/C & 0 & 0 & 0 \end{bmatrix}}_{\mathbf{A}} \tilde{\vec{x}} + \underbrace{\begin{bmatrix} V_{Cd}/L \\ V_{Cq}/L \\ V_{C0}/L \\ -I_{Ld}/C \\ -I_{Lq}/C \\ -I_{L0}/C \end{bmatrix}}_{\mathbf{B}} \tilde{\vec{u}} + \underbrace{\begin{bmatrix} 1/L & 0 & 0 \\ 0 & 1/L & 0 \\ 0 & 0 & 1/L \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}}_{\mathbf{E}} \tilde{\vec{v}}, \tag{5.48}$$

$$\tilde{\vec{y}} = \underbrace{\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix}}_{\mathbf{C}} \tilde{\vec{x}} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{D}} \tilde{\vec{u}}, \tag{5.49}$$

where

$$\begin{aligned} K_0^P &= (1 - K_0)\,, \\ \tilde{\vec{x}} &= \begin{bmatrix} \tilde{i}_{Ld} & \tilde{i}_{Lq} & \tilde{i}_{L0} & \tilde{v}_{Cd} & \tilde{v}_{Cq} & \tilde{v}_{C0} \end{bmatrix}^T, \\ \tilde{\vec{u}} &= \tilde{k}_0, \\ \tilde{\vec{v}} &= \begin{bmatrix} \tilde{v}_{Sd} & \tilde{v}_{Sq} & \tilde{v}_{S0} \end{bmatrix}^T, \end{aligned}$$

$$\tilde{\vec{y}} = \begin{bmatrix} \tilde{i}_{Sd} & \tilde{i}_{Sq} & \tilde{i}_{S0} \end{bmatrix}^T .$$

The DC state vectors, $\vec{I}_{Ldq0}$ and $\vec{V}_{Cdq0}$, are are given by,

$$\begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{L0} \end{bmatrix} = \begin{bmatrix} \left(-\left(1-K_0\right)^2 \omega C V_{Sq} + \omega^2 R C^2 V_{Sd} + \omega^3 L C^2 V_{Sq}\right)/\Psi \\ \left(\left(1-K_0\right)^2 \omega C V_{Sd} + \omega^2 R C^2 V_{Sq} - \omega^3 L C^2 V_{Sd}\right)/\Psi \\ 0 \end{bmatrix}, \tag{5.50}$$

$$\begin{bmatrix} V_{Cd} \\ V_{Cq} \\ V_{C0} \end{bmatrix} = \begin{bmatrix} \left(\left(1-K_0\right)^3 V_{Sd} + \left(1-K_0\right)\omega R C V_{Sq} - \left(1-K_0\right)\omega^2 L C V_{Sd}\right)/\Psi \\ \left(\left(1-K_0\right)^3 V_{Sq} - \left(1-K_0\right)\omega R C V_{Sd} - \left(1-K_0\right)\omega^2 L C V_{Sq}\right)/\Psi \\ V_{S0}/\left(1-K_0\right) \end{bmatrix}, \tag{5.51}$$

where

$$\Psi = \omega^4 L^2 C^2 + \omega^2 R^2 C^2 - 2\left(1-K_0\right)^2 \omega^2 L C + \left(1-K_0\right)^4 .$$

Equivalent circuit diagrams of the DQ0 small-signal model of the boost D-CAP are given in Figure 5.8.

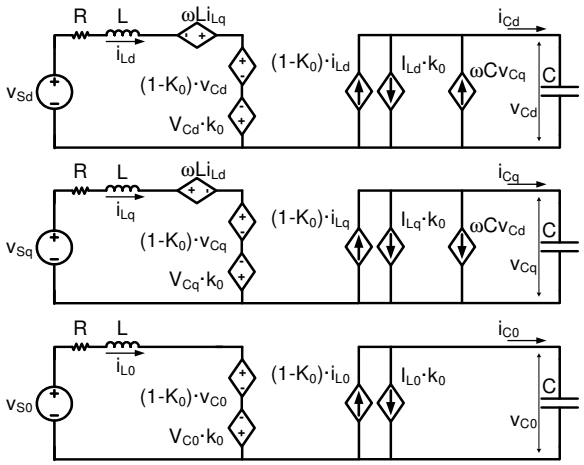


Figure 5.8: The linear small-signal DQ0 model of the boost D-CAP.

5.5.3 Buck-Boost D-CAP

The linear small-signal model of the buck-boost D-CAP using state-space representation is derived as follows:

$$\begin{aligned}\frac{d\tilde{\vec{x}}}{dt} = &\underbrace{\begin{bmatrix} -R/L & \omega & 0 & -K_0^P/L & 0 & 0 \\ -\omega & -R/L & 0 & 0 & -K_0^P/L & 0 \\ 0 & 0 & -R/L & 0 & 0 & -K_0^P/L \\ K_0^P/C & 0 & 0 & 0 & \omega & 0 \\ 0 & K_0^P/C & 0 & -\omega & 0 & 0 \\ 0 & 0 & K_0^P/C & 0 & 0 & 0 \end{bmatrix}}_{\mathbf{A}} \tilde{\vec{x}} \\ &+ \underbrace{\begin{bmatrix} (V_{Sd}+V_{Cd})/L \\ (V_{Sq}+V_{Cq})/L \\ (V_{S0}+V_{C0})/L \\ -I_{Ld}/C \\ -I_{Lq}/C \\ -I_{L0}/C \end{bmatrix}}_{\mathbf{B}} \tilde{\vec{u}} + \underbrace{\begin{bmatrix} K_0/L & 0 & 0 \\ 0 & K_0/L & 0 \\ 0 & 0 & K_0/L \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}}_{\mathbf{E}} \tilde{\vec{v}},\end{aligned} \tag{5.52}$$

$$\tilde{\vec{y}} = \underbrace{\begin{bmatrix} K_0 & 0 & 0 & 0 & 0 & 0 \\ 0 & K_0 & 0 & 0 & 0 & 0 \\ 0 & 0 & K_0 & 0 & 0 & 0 \end{bmatrix}}_{\mathbf{C}} \tilde{\vec{x}} + \underbrace{\begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{L0} \end{bmatrix}}_{\mathbf{D}} \tilde{\vec{u}}, \tag{5.53}$$

where

$$\begin{aligned} K_0^P &= (1-K_0), \\ \tilde{\vec{x}} &= \begin{bmatrix} \tilde{i}_{Ld} & \tilde{i}_{Lq} & \tilde{i}_{L0} & \tilde{v}_{Cd} & \tilde{v}_{Cq} & \tilde{v}_{C0} \end{bmatrix}^T, \\ \tilde{\vec{u}} &= \tilde{k}_0, \\ \tilde{\vec{v}} &= \begin{bmatrix} \tilde{v}_{Sd} & \tilde{v}_{Sq} & \tilde{v}_{S0} \end{bmatrix}^T, \end{aligned}$$

$$\tilde{\vec{y}} = \begin{bmatrix} \tilde{i}_{Sd} & \tilde{i}_{Sq} & \tilde{i}_{S0} \end{bmatrix}^T .$$

The DC state vectors $\vec{I}_{Ldq0}$ and $\vec{V}_{Cdq0}$ are given by,

$$\begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{L0} \end{bmatrix} = \begin{bmatrix} \left(K_0 \omega C \left(- \left(K_0^P \right)^2 V_{Sq} + \omega^2 LC V_{Sq} + \omega RC V_{Sd} \right) \right) / \Psi \\ \left(K_0 \omega C \left(\left(K_0^P \right)^2 V_{Sd} - \omega^2 LC V_{Sd} + \omega RC V_{Sq} \right) \right) / \Psi \\ 0 \end{bmatrix}, \tag{5.54}$$

$$\begin{bmatrix} V_{Cd} \\ V_{Cq} \\ V_{C0} \end{bmatrix} = \begin{bmatrix} \left(K_0 \left(K_0^P \right)^3 V_{Sd} + K_0 K_0^P C \left(\omega R V_{Sq} - \omega^2 L V_{Sd} \right) \right) / \Psi \\ \left(K_0 \left(K_0^P \right)^3 V_{Sq} - K_0 K_0^P C \left(\omega R V_{Sd} - \omega^2 L V_{Sq} \right) \right) / \Psi \\ V_{S0} K_0 / K_0^P \end{bmatrix}, \tag{5.55}$$

where

$$\Psi = \omega^4 L^2 C^2 + \omega^2 R^2 C^2 - 2 \left(K_0^P \right)^2 \omega^2 LC + \left(K_0^P \right)^4 ,$$

$$K_0^P = 1 - K_0 .$$

Equivalent circuit diagrams representing the DQ0 small-signal model of the buck-boost D-CAP are given in Figure 5.9.

5.6 Justifications for the Selection of the Duty Function

The form of the duty-cycle function, $d(t)$, used in controlling the semiconductor devices in the DVHC converters has previously been described by Equation (3.6) and listed here for reference:

$$d(t) = K_0 + K_2 \sin(2\omega t + \phi_2) + K_4 \sin(4\omega t + \phi_4) + ... \tag{3.6}$$

The two primary assumptions made in the derivation of the small-signal model of the DVHC converters has been that,

1. each of the three phases is controlled with the same duty command, and
2. the duty function is devoid of any even harmonic terms, $d_a(t) = d_b(t) = d_c(t) = k_0$.

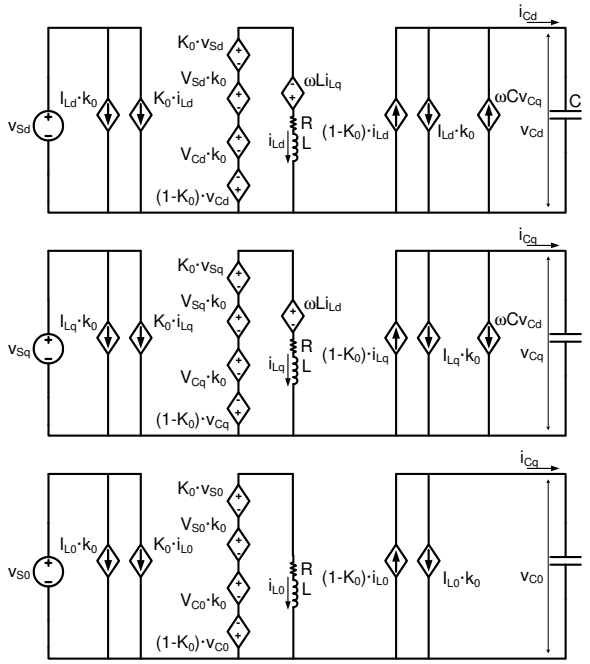


Figure 5.9: The linear small-signal DQ0 model of the buck-boost D-CAP.

If the duty function for each of the three phases is different, the duty matrix, d_{abc}, in the ABC average models of the buck, boost and buck-boost topologies is given by:

$$d_{abc} = \begin{bmatrix} d_a & 0 & 0 \\ 0 & d_b & 0 \\ 0 & 0 & d_c \end{bmatrix} \tag{5.56}$$

Converting from the stationary to the synchronous reference frame, the following duty function is obtained:

$$d_{dq0} = T^{-1}_{dq0/abc} d_{abc} T_{dq0/abc} = \begin{bmatrix} d_{d-d} & d_{d-q} & d_{d-0} \\ d_{q-d} & d_{q-q} & d_{q-0} \\ d_{0-d} & d_{0-q} & d_{0-0} \end{bmatrix}, \tag{5.57}$$

where

$$d_{d-d} = \frac{d_b}{2} + \frac{d_c}{2} + \frac{1}{6}\left(2d_a - d_b - d_c\right)\cos\left(2\omega t\right) - \frac{\sqrt{3}}{6}\left(d_b - d_c\right)\sin\left(2\omega t\right),$$
$$d_{d-q} = \frac{1}{3}\left(\frac{d_b}{2} - d_a + \frac{d_c}{2}\right)\sin\left(2\omega t\right) - \frac{\sqrt{3}}{6}\left(d_b - d_c\right)\cos\left(2\omega t\right),$$

$$d_{d-0} = \frac{\sqrt{2}}{3}\left(d_a - \frac{d_b}{2} - \frac{d_c}{2}\right)\cos(\omega t) + \frac{\sqrt{6}}{6}(d_b - d_c)\sin(\omega t),$$

$$d_{q-d} = d_{d-q},$$

$$d_{q-q} = \frac{2d_a}{3} + \frac{d_b}{6} + \frac{d_c}{6} - \frac{1}{6}(2d_a - d_b - d_c)\cos(2\omega t) + \frac{\sqrt{3}}{6}(d_b - d_c)\sin(2\omega t),$$

$$d_{q-0} = \frac{\sqrt{2}}{3}\left(\frac{d_b}{2} - d_a + \frac{d_c}{2}\right)\sin(\omega t) + \frac{\sqrt{6}}{6}(d_b - d_c)\cos(\omega t),$$

$$d_{0-d} = d_{d-0},$$

$$d_{0-q} = d_{q-0},$$

$$d_{0-0} = \frac{d_a}{3} + \frac{d_b}{3} + \frac{d_c}{3}.$$

The results indicate that if the constant terms in all three phases are not the same, sinusoidal terms in the synchronous reference frame are induced. In order to model a linear time-invariant plant, all the terms have to be resolved as DC.

For the same reason, the even harmonic terms are not considered as part of the duty function, because when the transformation, $T^{-1}_{dq0/abc} d_{abc} T_{dq0/abc}$, is applied to the duty function to go from stationary to synchronous reference frame, the resulting duty function matrix in the DQ0 space contains multiple sinusoidal components that do not resolve to DC.

Thus, the only way to derive the LTI model of the plant is to assume the same constant duty function for all three phases, as has been done in this work.

As mentioned earlier, while the harmonic components cannot be addressed with this approach, a workaround to the restrictions that all the duty terms be the same for all three phases, is to model the other two phases as 'virtual', existing only to enable transformation from the stationary to synchronous reference frame. In order to model all three phases for a three-phase implementation, nine total phases are considered as part of the modeling, with six of the phases as virtual.

5.7 Transfer Functions

The transfer functions are derived by applying the Laplace transform to the state-space model of the three systems and extracting the functions expressed as the ratio of two variables; where the one on the top is considered to be the 'output' and the one on the bottom is the 'input'.

Each of the three state-space models has been written in the form:

$$\frac{d\tilde{\vec{x}}}{dt} = \mathbf{A}\tilde{\vec{x}} + \mathbf{B}\tilde{\vec{u}} + \mathbf{E}\tilde{\vec{v}}, \tag{5.58}$$

$$\tilde{\vec{y}} = \mathbf{C}\tilde{\vec{x}} + \mathbf{D}\tilde{\vec{u}}, \tag{5.59}$$

where

$$\tilde{\vec{x}} = \begin{bmatrix} \tilde{i}_{Ld} & \tilde{i}_{Lq} & \tilde{i}_{L0} & \tilde{v}_{Cd} & \tilde{v}_{Cq} & \tilde{v}_{C0} \end{bmatrix}^T,$$

$$\tilde{\vec{u}} = \tilde{k_0},$$

$$\tilde{\vec{v}} = \begin{bmatrix} \tilde{v}_{Sd} & \tilde{v}_{Sq} & \tilde{v}_{S0} \end{bmatrix}^T,$$

$$\tilde{\vec{y}} = \begin{bmatrix} \tilde{i}_{Sd} & \tilde{i}_{Sq} & \tilde{i}_{S0} \end{bmatrix}^T.$$

For the D-CAP, the output variables of interests are the injected or source-side currents, $\tilde{\vec{y}} = \begin{bmatrix} \tilde{i}_{Sd} & \tilde{i}_{Sq} & \tilde{i}_{S0} \end{bmatrix}^T$. The input variables that will be perturbed to observe the resulting behavior on the output variables are typically selected to be $\tilde{\vec{u}} = \tilde{k}_0$ and $\tilde{\vec{v}} = [\tilde{v}_{Sd}\ \tilde{v}_{Sq}\ \tilde{v}_{S0}]^T$.

Applying Laplace transform to Equations (5.58)-(5.58) and rearranging the resulting expressions in terms of only $\tilde{\vec{y}}(s)$, $\tilde{\vec{u}}(s)$ and $\tilde{\vec{v}}(s)$, the following generalized expression is obtained:

$$\tilde{\vec{y}}(s) = \left(\mathbf{C}\left(s\mathrm{I} - \mathbf{A}\right)^{-1}\mathbf{B} + \mathbf{D}\right)\tilde{\vec{u}}(s) + \mathbf{C}\left(s\mathrm{I} - \mathbf{A}\right)^{-1}\mathbf{E}\tilde{\vec{v}}(s) \tag{5.60}$$

5.7.1 Buck D-CAP

The open-loop transfer functions for the buck D-CAP are derived using the expression given by Equation (5.60). The transfer functions relating the D and Q component of

the output current for a perturbation in the duty cycle are given by,

$$\frac{\tilde{i}_{Sd}(s)}{\tilde{k}_0(s)} = \frac{\left(P_4^d s^4 + P_3^d s^3 + P_2^d s^2 + P_1^d s + P_0^d\right)}{\Gamma}, \tag{5.61}$$

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{k}_0(s)} = \frac{\left(P_4^q s^4 + P_3^q s^3 + P_2^q s^2 + P_1^q s + P_0^q\right)}{\Gamma}. \tag{5.62}$$

For perturbations in the D, Q, and 0 components of the input voltage and their effect upon the D and Q component of the output current are given by,

$$\frac{\tilde{i}_{Sd}(s)}{\tilde{v}_{Sd}(s)} = \frac{K_0^2 LC^2 s^3 + K_0^2 RC^2 s^2 + \left(K_0^2\omega^2 LC^2 + K_0^2 C\right)s + K_0^2\omega^2 RC^2}{\Gamma}, \tag{5.63}$$

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{v}_{Sq}(s)} = -\frac{K_0^2\omega LC^2 s^2 + K_0^2\omega^3 LC^2 - K_0^2\omega C}{\Gamma}, \tag{5.64}$$

$$\frac{\tilde{i}_{Sd}(s)}{\tilde{v}_{Sq}(s)} = \frac{K_0^2\omega LC^2 s^2 + K_0^2\omega^3 LC^2 - K_0^2\omega C}{\Gamma}, \tag{5.65}$$

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{v}_{Sd}(s)} = \frac{K_0^2 LC^2 s^3 + K_0^2 RC^2 s^2 + \left(K_0^2\omega^2 LC^2 + K_0^2 C\right)s + K_0^2\omega^2 RC^2}{\Gamma}, \tag{5.66}$$

$$\frac{\tilde{i}_{S0}(s)}{\tilde{v}_{S0}(s)} = \frac{K_0^2 Cs}{LCs^2 + RCs - 1}. \tag{5.67}$$

where

$$P_4^d = L^2C^2 I_{Ld},$$

$$P_3^d = 2RLC^2 I_{Ld} + K_0 LC^2 V_{Sd},$$

$$P_2^d = 2\omega^2 L^2C^2 I_{Ld} + K_0\omega LC^2 V_{Sq} + R^2C^2 I_{Ld} + K_0 RC^2 V_{Sd} + 2LCI_{Ld},$$

$$P_1^d = K_0 CV_{Sd} + 2RCI_{Ld} + K_0\omega^2 LC^2 V_{Sd} + 2\omega^2 RLC^2 I_{Ld},$$

$$P_0^d = -2\omega^2 LCI_{Ld} - K_0\omega CV_{Sq} + \omega^4 L^2C^2 I_{Ld} + \omega^2 R^2C^2 I_{Ld} + K_0\omega^3 LC^2 V_{Sq} + K_0\omega^2 RC^2 V_{Sd} + I_{Ld},$$

$$P_4^q = L^2C^2 I_{Lq},$$

$$P_3^q = 2RLC^2 I_{Lq} + K_0 LC^2 V_{Sq},$$

$$P_2^q = 2\omega^2 L^2C^2 I_{Lq} - K_0\omega LC^2 V_{Sd} + R^2C^2 I_{Lq} + K_0 RC^2 V_{Sq} + 2LCI_{Lq},$$

$$P_1^q = K_0 CV_{Sq} + 2RCI_{Lq} + K_0\omega^2 LC^2 V_{Sq} + 2\omega^2 RLC^2 I_{Lq},$$

$$
\begin{aligned}
P_0^q &= -2\omega^2 LCI_{Lq} + K_0\omega CV_{Sd} + \omega^4 L^2C^2 I_{Lq} + \omega^2 R^2C^2 I_{Lq} \\
&\quad - K_0\omega^3 LC^2 V_{Sd} + K_0\omega^2 RC^2 V_{Sq} + I_{Lq}, \\
\Gamma &= L^2C^2 s^4 + 2RLC^2 s^3 + \left(2\omega^2 L^2C^2 + R^2C^2 + 2LC\right) s^2 \\
&\quad + \left(2\omega^2 RLC^2 + 2RC\right) s + \omega^4 L^2C^2 + \omega^2 R^2C^2 - \omega^2 2LC + 1.
\end{aligned}
$$

5.7.2 Boost D-CAP

The open-loop transfer functions for the boost D-CAP are similarly derived using the expression given by Equation (5.60). The transfer functions relating the D and Q component of the output current to the duty-cycle perturbations are given by,

$$\frac{\tilde{i}_{Sd}(s)}{\tilde{k}_0(s)} = \frac{P_3^d s^3 + P_2^d s^2 + P_1^d s + P_0^d}{\Gamma}, \tag{5.68}$$

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{k}_0(s)} = \frac{P_3^q s^3 + P_2^q s^2 + P_1^q s + P_0^q}{\Gamma}. \tag{5.69}$$

The ones relating the output current to the D, Q, and 0 component of the input voltage are:

$$\frac{\tilde{i}_{Sd}(s)}{\tilde{v}_{Sd}(s)} = \frac{LC^2 s^3 + RC^2 s^2 + \left(\omega^2 LC^2 + \left(K_0^P\right)^2 C\right) s + \omega^2 RC^2}{\Gamma}, \tag{5.70}$$

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{v}_{Sd}(s)} = -\frac{\omega LC^2 s^2 + \omega^3 LC^2 - \left(K_0^P\right)^2 \omega C}{\Gamma}, \tag{5.71}$$

$$\frac{\tilde{i}_{Sd}(s)}{\tilde{v}_{Sq}(s)} = \frac{\omega LC^2 s^2 + \omega^3 LC^2 - \left(K_0^P\right)^2 \omega C}{\Gamma}, \tag{5.72}$$

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{v}_{Sq}(s)} = \frac{LC^2 s^3 + RC^2 s^2 + \left(\omega^2 LC^2 + \left(K_0^P\right)^2 C\right) s + \omega^2 RC^2}{\Gamma}, \tag{5.73}$$

$$\frac{\tilde{i}_{S0}(s)}{\tilde{v}_{S0}(s)} = \frac{Cs}{LCs^2 + RCs + \left(K_0^P\right)^2}, \tag{5.74}$$

where

$$
\begin{aligned}
P_3^d &= LC^2 V_{Cd}, \\
P_2^d &= RC^2 V_{Cd} + \omega LC^2 V_{Cq} + K_0^P LCI_{Ld},
\end{aligned}
$$

$$
\begin{aligned}
P_1^d &= \omega^2 LC^2 V_{Cd} + \left(K_0^P\right)^2 CV_{Cd} + 2K_0^P \omega LCI_{Lq} + K_0^P RCI_{Ld}, \\
P_0^d &= -\left(K_0^P\right)^2 \omega CV_{Cq} + \omega^3 LC^2 V_{Cq} + \omega^2 RC^2 V_{Cd} - K_0^P \omega^2 LCI_{Ld} \\
&\quad + K_0^P \omega RCI_{Lq} + \left(K_0^P\right)^3 I_{Ld}, \\
P_3^q &= LC^2 V_{Cq}, \\
P_2^q &= RC^2 V_{Cq} - \omega LC^2 V_{Cd} + K_0^P LCI_{Lq}, \\
P_1^q &= \omega^2 LC^2 V_{Cq} + \left(K_0^P\right)^2 CV_{Cq} - 2K_0^P \omega LCI_{Ld} + K_0^P RCI_{Lq}, \\
P_0^q &= \left(K_0^P\right)^2 \omega CV_{Cd} - \omega^3 LC^2 V_{Cd} + \omega^2 RC^2 V_{Cq} - K_0^P \omega^2 LCI_{Lq} \\
&\quad - K_0^P \omega RCI_{Ld} + \left(K_0^P\right)^3 I_{Lq}, \\
\Gamma &= L^2 C^2 s^4 + 2RLC^2 s^3 + \left(2\omega^2 L^2 C^2 + R^2 C^2 + 2\left(K_0^P\right)^2 LC\right) s^2 \\
&\quad + \left(2\omega^2 RLC^2 + 2\left(K_0^P\right)^2 RC\right) s + \omega^4 L^2 C^2 + \omega^2 R^2 C^2 \\
&\quad - 2\left(K_0^P\right)^2 \omega^2 LC + \left(K_0^P\right)^4, \\
K_0^P &= 1 - K_0.
\end{aligned}
$$

5.7.3 Buck-Boost D-CAP

The open-loop transfer functions for the buck-boost D-CAP are also similarly derived. The transfer functions relating the output current to the perturbation in the duty cycle are:

$$\frac{\tilde{i}_{Sd}(s)}{\tilde{k}_0(s)} = \frac{\left(P_4^d s^4 + P_3^d s^3 + P_2^d s^2 + P_1^d s + P_0^d\right)}{\Gamma}, \tag{5.75}$$

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{k}_0(s)} = \frac{\left(P_4^q s^4 + P_3^q s^3 + P_2^q s^2 + P_1^q s + P_0^q\right)}{\Gamma}. \tag{5.76}$$

The transfer functions modeling the dynamics of the output current due to perturbation in the input volatage are:

$$\frac{\tilde{i}_{Sd}(s)}{\tilde{v}_{Sd}(s)} = \frac{K_0^2 LC^2 s^3 + K_0^2 RC^2 s^2 + \left(K_0^2 \omega^2 LC^2 + K_0^2\left(K_0^P\right)^2 C\right) s + K_0^2 \omega^2 RC^2}{\Gamma}, \tag{5.77}$$

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{v}_{Sd}(s)} = -\frac{K_0^2\omega LC^2s^2 + K_0^2\omega^3LC^2 - K_0^2\left(K_0^P\right)^2\omega C}{\Gamma}, \tag{5.78}$$

$$\frac{\tilde{i}_{Sd}(s)}{\tilde{v}_{Sq}(s)} = \frac{K_0^2\omega LC^2s^2 + K_0^2\omega^3LC^2 - K_0^2\left(K_0^P\right)^2\omega C}{\Gamma}, \tag{5.79}$$

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{v}_{Sq}(s)} = \frac{K_0^2LC^2s^3 + K_0^2RC^2s^2 + \left(K_0^2\omega^2LC^2 + K_0^2\left(K_0^P\right)^2C\right)s + K_0^2\omega^2RC^2}{\Gamma}, \tag{5.80}$$

$$\frac{\tilde{i}_{S0}(s)}{\tilde{v}_{S0}(s)} = \frac{K_0^2Cs}{LCs^2 + RCs + \left(K_0^P\right)^2}, \tag{5.81}$$

where

$$\begin{aligned}
P_4^d &= L^2C^2I_{Ld},\\
P_3^d &= 2RLC^2I_{Ld} + K_0LC^2\left(V_{Sd} + V_{Cd}\right),\\
P_2^d &= 2\omega^2L^2C^2I_{Ld} + K_0\omega LC^2\left(V_{Sq} + V_{Cq}\right) + R^2C^2I_{Ld}\\
&\quad + K_0RC^2\left(V_{Sd} + V_{Cd}\right) + 2\left(K_0^P\right)^2LCI_{Ld} + K_0K_0^PLCI_{Ld},\\
P_1^d &= K_0\left(K_0^P\right)^2C\left(V_{Sd} + V_{Cd}\right) + 2\left(K_0^P\right)^2RCI_{Ld} + K_0\omega^2LC^2\left(V_{Sd} + V_{Cd}\right)\\
&\quad + 2\omega^2RLC^2I_{Ld} + K_0K_0^PRCI_{Ld} + 2K_0K_0^P\omega LCI_{Lq},\\
P_0^d &= K_0\left(K_0^P\right)^3I_{Ld} + \omega^4L^2C^2I_{Ld} + \omega^2R^2C^2I_{Ld} - K_0\left(K_0^P\right)^2\omega C\left(V_{Sq} + V_{Cq}\right)\\
&\quad - 2\left(K_0^P\right)^2\omega^2LCI_{Ld} + K_0\omega^3LC^2\left(V_{Sq} + V_{Cq}\right) + K_0\omega^2RC^2\left(V_{Sd} + V_{Cd}\right)\\
&\quad + K_0K_0^P\omega RCI_{Lq} - K_0K_0^P\omega^2LCI_{Ld} + \left(K_0^P\right)^4I_{Ld},\\
P_4^q &= L^2C^2I_{Ld},\\
P_3^q &= 2RLC^2I_{Lq} + K_0LC^2\left(V_{Sq} + V_{Cq}\right),\\
P_2^q &= 2\omega^2L^2C^2I_{Lq} - K_0\omega LC^2\left(V_{Sd} + V_{Cd}\right) + R^2C^2I_{Lq}\\
&\quad + K_0RC^2\left(V_{Sq} + V_{Cq}\right) + 2\left(K_0^P\right)^2LCI_{Lq} + K_0K_0^PLCI_{Lq},\\
P_1^q &= K_0\left(K_0^P\right)^2C\left(V_{Sq} + V_{Cq}\right) + 2\left(K_0^P\right)^2RCI_{Lq} + K_0\omega^2LC^2\left(V_{Sq} + V_{Cq}\right)\\
&\quad + 2\omega^2RLC^2I_{Lq} + K_0K_0^PRCI_{Lq} - 2K_0K_0^P\omega LCI_{Ld},
\end{aligned}$$

$$
\begin{aligned}
P_0^q = {} & K_0\left(K_0^P\right)^3 I_{Lq} + \omega^4 L^2 C^2 I_{Lq} + \omega^2 R^2 C^2 I_{Lq} + K_0\left(K_0^P\right)^2 \omega C\left(V_{Sd} + V_{Cd}\right) \\
& - 2\left(K_0^P\right)^2 \omega^2 LC I_{Lq} - K_0\omega^3 LC^2\left(V_{Sd} + V_{Cd}\right) + K_0\omega^2 RC^2\left(V_{Sq} + V_{Cq}\right) \\
& - K_0 K_0^P \omega RC I_{Ld} - K_0 K_0^P \omega^2 LC I_{Lq} + \left(K_0^P\right)^4 I_{Lq}, \\
\Gamma = {} & L^2C^2s^4 + 2RLC^2s^3 + \left(2\omega^2 L^2C^2 + R^2C^2 + 2\left(K_0^P\right)^2 LC\right)s^2 \\
& + \left(2\omega^2 RLC^2 + 2\left(K_0^P\right)^2 RC\right)s + \omega^4 L^2C^2 + \omega^2 R^2C^2 \\
& - 2\left(K_0^P\right)^2 \omega^2 LC + \left(K_0^P\right)^4.
\end{aligned}
$$

5.7.4 Example Case Scenario

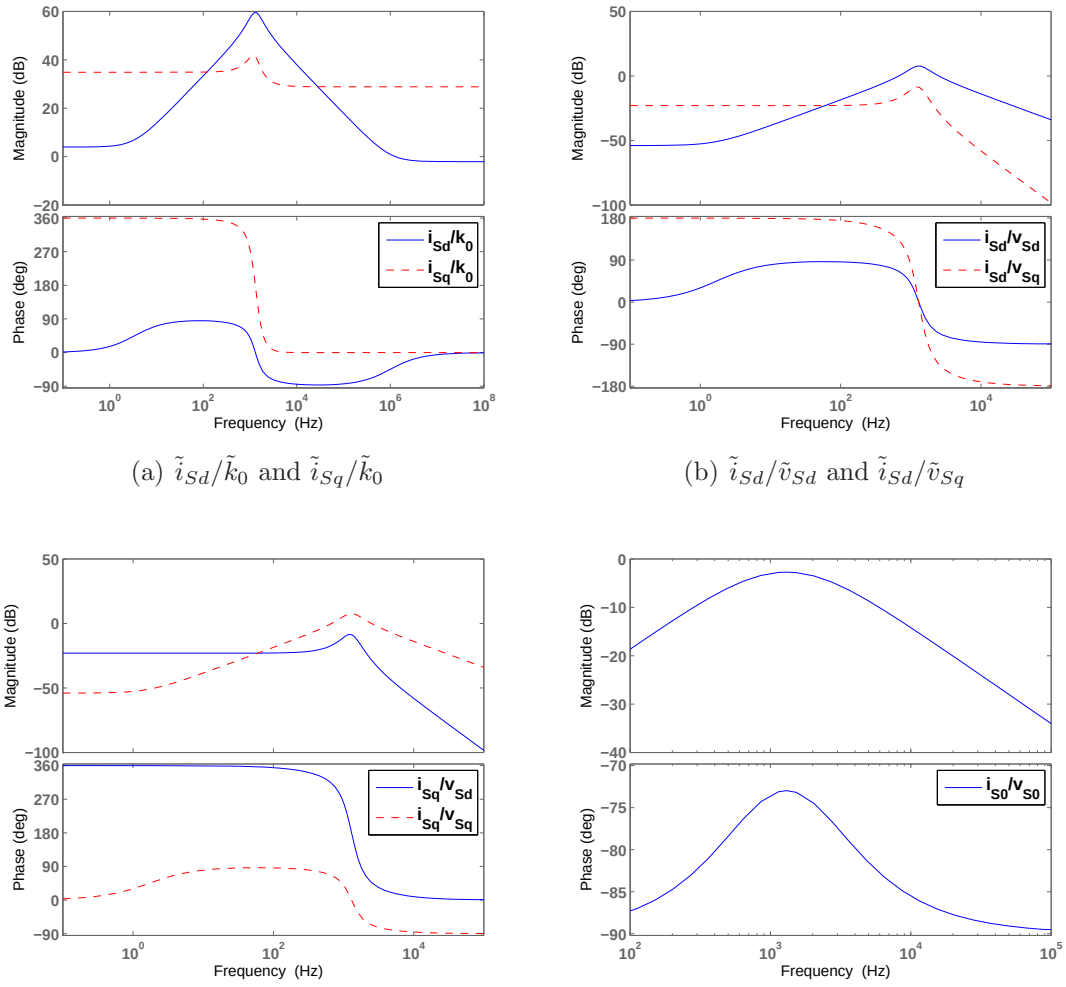
The seven transfer functions for each of the three configurations of the D-CAP are plotted based on the operating conditions and component values specified in Table 5.2. These transfer functions are given by Figures 5.10, 5.11, and 5.12, for the buck, boost and buck-boost D-CAP, respectively.

Table 5.2: The operating conditions and component values used in plotting the example transfer functions.

Operating Condition / Component	Value	Unit	Description
$[V_{Sd}\ V_{Sq}\ V_{S0}]$	$[480\sqrt{\frac{2}{3}}\ 0\ 0]$	V	Source voltage
C	1	mF	Main capacitor
L	100	μH	Switching inductor
R	0.1	Ω	Parasitic resistance
ω	$2\pi 60$	rad/s	Line frequency
K_0	0.5	-	Buck duty
	0.2	-	Boost duty
	0.4	-	Buck-boost duty

5.8 Conclusions

The average models of the buck, boost and buck-boost D-CAP are derived in the stationary (ABC) and synchronous reference frames (DQ0). The transformation to



(a) $\tilde{i}_{Sd}/\tilde{k}_0$ and $\tilde{i}_{Sq}/\tilde{k}_0$

(b) $\tilde{i}_{Sd}/\tilde{v}_{Sd}$ and $\tilde{i}_{Sd}/\tilde{v}_{Sq}$

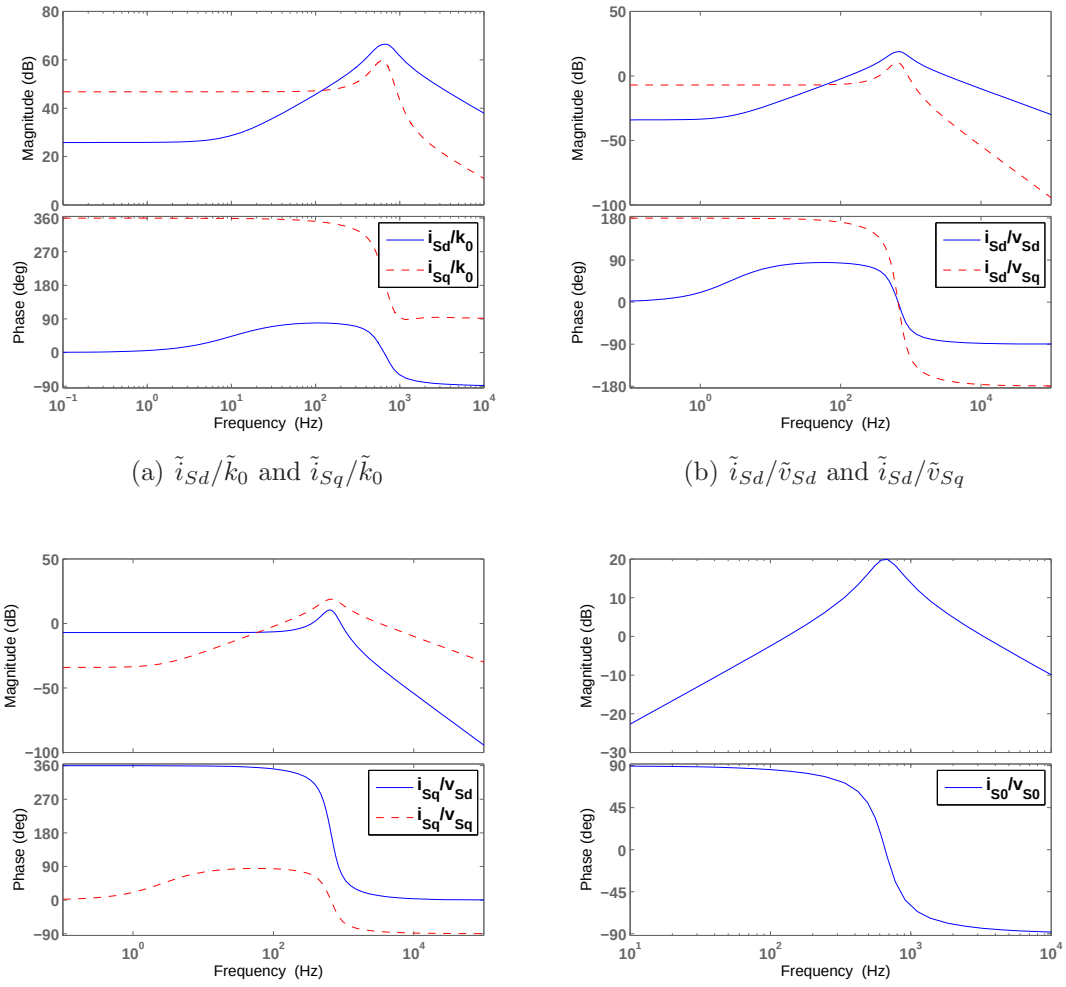
(c) $\tilde{i}_{Sq}/\tilde{v}_{Sd}$ and $\tilde{i}_{Sq}/\tilde{v}_{Sq}$

(d) $\tilde{i}_{S0}/\tilde{v}_{S0}$

Figure 5.10: The relevant transfer functions for the buck D-CAP.

the synchronous reference frame requires that all the quantities are either DC or are at a single frequency. Because of this, even harmonic modulation (EHM) of the switching devices is not considered for developing the models in the DQ0 coordinate-space.

The average DQ0 models are perturbed around a DC quiescent point in order to derive the state-space representation of the small-signal models. The transfer functions describing the dynamics of the output current due to a perturbation in the duty cycle or the grid voltage are subsequently extracted from these small-signal models. These functions are used to examine susceptibility to noise and disturbances,



(a) $\tilde{i}_{Sd}/\tilde{k}_0$ and $\tilde{i}_{Sq}/\tilde{k}_0$

(b) $\tilde{i}_{Sd}/\tilde{v}_{Sd}$ and $\tilde{i}_{Sd}/\tilde{v}_{Sq}$

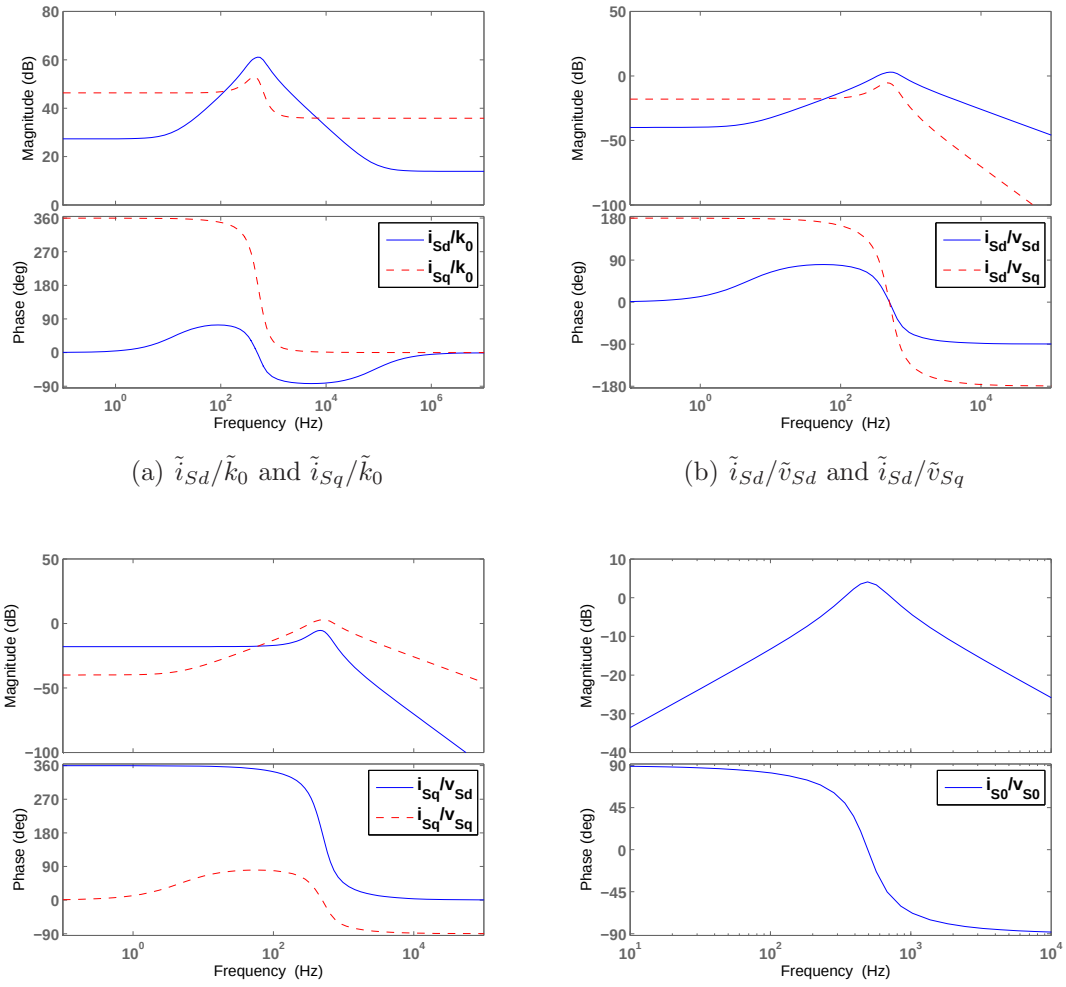
(c) $\tilde{i}_{Sq}/\tilde{v}_{Sd}$ and $\tilde{i}_{Sq}/\tilde{v}_{Sq}$

(d) $\tilde{i}_{S0}/\tilde{v}_{S0}$

Figure 5.11: The relevant transfer functions for the boost D-CAP.

and in turn, to design effective closed-loop controllers to mitigate their effects and achieve the desired control objectives in a robust and stable manner.

The derivations of the small-signal models are predicated upon the transformation of the converters from stationary to synchronous reference frame. While the D-CAP will typically be installed onto a three-phase grid, the implementation itself will be on a single-phase basis and as such, each phase will be independently controlled to facilitate unbalanced and asymmetrical compensation. However, the



(a) $\tilde{i}_{Sd}/\tilde{k}_0$ and $\tilde{i}_{Sq}/\tilde{k}_0$

(b) $\tilde{i}_{Sd}/\tilde{v}_{Sd}$ and $\tilde{i}_{Sd}/\tilde{v}_{Sq}$

(c) $\tilde{i}_{Sq}/\tilde{v}_{Sd}$ and $\tilde{i}_{Sq}/\tilde{v}_{Sq}$

(d) $\tilde{i}_{S0}/\tilde{v}_{S0}$

Figure 5.12: The relevant transfer functions for the buck-boost D-CAP.

required transformation to the synchronous reference frame does not produce constant or DC quantities with an asymmetrically controlled D-CAP system, even with constant duty cycles. For that reason, each phase is modeled independently from the other two phases with its own two virtual phases that are perfect mirrors of the actual phase but phase-shifted by 120 degrees. In total, to model all three phases, three sets of three-phase circuits, or total of nine circuits, are required. For those rare applications that require balanced compensation, one set of three-phase circuits is adequate.

The synchronous reference frame average and small-signal models have three components: direct (D), quadrature (Q), and zero-sequence component (0). The source or grid voltage is typically aligned with the direct axis, while the injected current, under purely VAR compensation, subsequently falls on the quadrature axis. For modeling the single-phase systems, the zero-sequence component may be ignored entirely as that component literally has 'zero' currents and voltages under balanced conditions, which is always the case with two mirrored virtual phases.

CHAPTER VI

FREQUENCY-DOMAIN MODELING

6.1 Introduction

The simultaneous existence of multiple harmonics in the operation of the DVHC converters in active filter applications prevents the development of linear time-invariant models of the plants. An alternate approach is to model the plants in the frequency domain where the characteristics of the passive elements like resistors, inductors, and capacitors, functionality of active elements such as IGBTs and diodes, and measurable energy indexes like voltages and currents of a converter are described at discrete frequency points ranging from the lowest frequency of interest to the highest. By representing the response or behavior of the converter over a range of frequency or harmonics (multiples of the line frequency) in a matrix form, a complete steady-state operating model of the converter can be obtained.

The frequency model of the buck, boost and buck-boost Dynamic Capacitor are derived in this chapter. Although D-CAP is used to derive the models, the approach can easily be extended to the Dynamic Inductor and Dynamic Resistor as well by simply replacing the capacitor with either an inductor or a resistor and re-deriving the corresponding frequency model of the passive component.

The models are initially derived without considering the input filters so as to not overly complicate the discussion. Their impact is assessed as a second step.

A numerical gradient approach using the Newton/Rapshon algorithm is also presented in order to inversely calculate the duty cycle for a reference current with specific harmonic components.

6.2 Overview of the Modeling Approach

The voltages and currents in the converter are represented using Fourier series where arbitrary waveforms that are integrable and 2π-periodic undergo decomposition into the sum of purely sine and cosine terms at the various harmonics, as given by,

$$f(\omega t) = \frac{a_0}{2} + \sum_{h=1}^{\infty} [a_h \sin(h\omega t) + b_h \cos(h\omega t)], \tag{6.1}$$

where

$$a_h = \frac{1}{\pi} \int_0^{2\pi} f(\omega t) \sin(h\omega t)\, d(\omega t), \tag{6.2}$$

$$b_h = \frac{1}{\pi} \int_0^{2\pi} f(\omega t) \cos(h\omega t)\, d(\omega t). \tag{6.3}$$

Therefore, these waveforms are described entirely by their Fourier coefficients, a_h and b_h, organized as a one-dimensional matrix and listed in an increasing harmonic order,

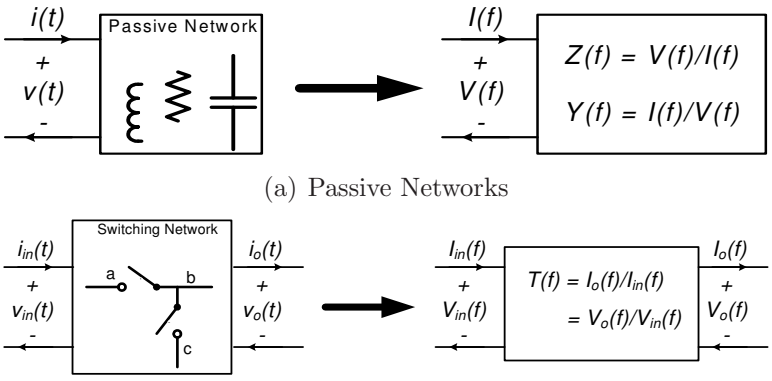
$$V = \left[\underbrace{V_1 ... V_{N_H}}_{cos} \underbrace{V_1 ... V_{N_H}}_{sin} \right], \tag{6.4}$$

$$I = \left[\underbrace{I_1 ... I_{N_H}}_{cos} \underbrace{I_1 ... I_{N_H}}_{sin} \right], \tag{6.5}$$

for voltage and current, respectively. The first set of N_H coefficients are for the cosine terms, and the second set of N_H coefficients are for the sine terms. The characteristic frequencies typically only exist at odd harmonics for power system applications, so the even harmonics are not considered.

The frequency domain models of the DVHCs are derived for each of the components in the converter, as exemplified by Figure 6.1. The characteristics and the relationships between the voltages and the currents in the switching network and the passive components are defined at each frequency of interest. For a DVHC converter, the forcing function is the line voltage, V_S, while the variable of interest is the current, I_S, drawn or injected by the converter from the line for VAR and harmonic

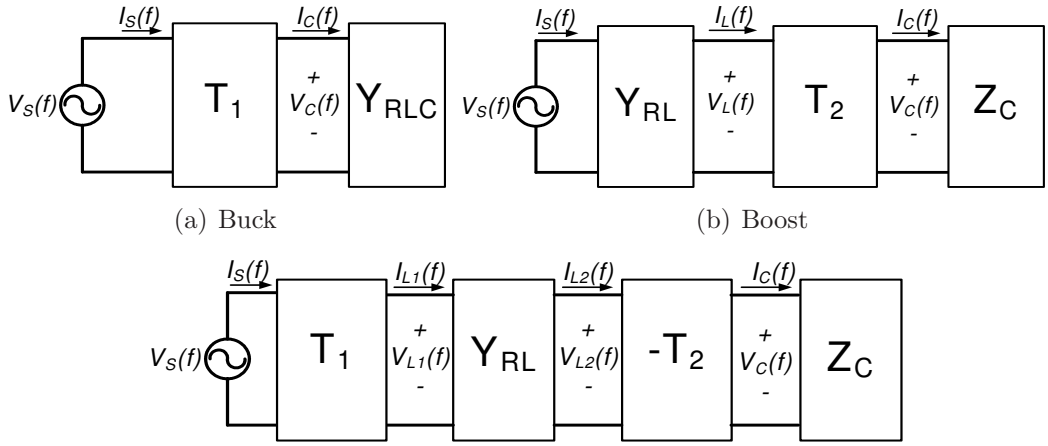
compensation. The previously derived stationary-reference-frame average models are converted to frequency-domain models for the buck, boost, and buck-boost D-CAP as shown in Figure 6.2. The switching cell models, T_1 and T_2, correspond to the duty function, $d(t)$, and its complement, $1 - d(t)$, respectively.



(a) Passive Networks

(b) Switching Networks

Figure 6.1: Frequency-domain representations of the passive and the active components.



(a) Buck

(b) Boost

(c) Buck-Boost

Figure 6.2: The depictions of the frequency-domain models for the three configurations of the D-CAP.

6.3 Modeling of the Passive Components

The frequency models of the passive components can be represented as either an impedance matrix, Z, where $V = ZI$, or as an admittance matrix, Y, where $I = YV$. Here, the Z and Y describe the transformation the current or voltages undergo through a passive network with a particular combination of a capacitor, C, inductor, L, and/or a resistor, R.

For the frequency models of the passive components depicted in Figure 6.2, the admittance and impedance matrices are derived at each harmonic number, h, where $h = 2n-1$ for $n = [1, 2, 3, ..., N_H]$. The admittance matrix, Y_{RLC}, describing the series-connected switching inductor, L, the main capacitor, C, and the parasitic resistance, R, for the buck D-CAP is given by,

$$Y_{RLC} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}_{2N_H \times 2N_H}, \tag{6.6}$$

where

$$\begin{aligned} Y_{11}(n,n) &= Y_{22}(n,n) = \Re\left(y_{RLC}(n)\right), \\ Y_{12}(n,n) &= \Im\left(y_{RLC}(n)\right), \\ Y_{21}(n,n) &= -\Im\left(y_{RLC}(n)\right), \\ y_{RLC}(n) &= j\frac{2\pi 60hC}{1 + j2\pi 60hRC - (2\pi 60h)^2 LC}. \end{aligned}$$

The impedance model for the main capacitor, C, in the boost and buck-boost is,

$$Z_C = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}_{2N_H \times 2N_H}, \tag{6.7}$$

where

$$Z_{11}(n,n) = Z_{22}(n,n) = \Re\left(z_C(n)\right),$$

$$
\begin{aligned}
Z_{12}(n,n) &= \Im\left(z_C(n)\right), \\
Z_{21}(n,n) &= -\Im\left(z_C(n)\right), \\
z_C(n) &= -j\frac{1}{2\pi 60hC}.
\end{aligned}
$$

And the admittance model for the switching inductor, L, with series parasitic resistance, R, is given by,

$$
Y_{RL} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}_{2N_H \times 2N_H}, \tag{6.8}
$$

where

$$
\begin{aligned}
Y_{11}(n,n) &= Y_{22}(n,n) = \Re\left(y_{RL}(n)\right), \\
Y_{12}(n,n) &= \Im\left(y_{RL}(n)\right), \\
Y_{21}(n,n) &= -\Im\left(y_{RL}(n)\right), \\
y_{RL}(n) &= \frac{1}{R + j2\pi 60hL}.
\end{aligned}
$$

6.4 Modeling of the Switching Cell

In deriving the model of the switching cell, each even harmonics in the duty-cycle function are represented as a sum of pure sine and cosine terms without phase-shifts:

$$
\begin{aligned}
d(t) = K_0 &+ K_{2c}\cos(2\omega t) + K_{2s}\sin(2\omega t) \\
&+ K_{4c}\cos(4\omega t) + K_{4s}\sin(4\omega t) + ...
\end{aligned} \tag{6.9}
$$

When a voltage or current of h-th harmonic,

$$
u(h\omega t) = U_{hc}\cos(h\omega t) + U_{hs}\sin(h\omega t),
$$

is multiplied by the g-th even harmonic term in the duty function,

$$
d(g\omega t) = K_{nc}\cos(g\omega t) + K_{gs}\sin(g\omega t),
$$

the resulting product, collected based on the harmonic number and sine/cosine terms, is given by,

$$\begin{aligned} d\left(g\omega t\right)\cdot u\left(h\omega t\right) = & \left[\frac{1}{2}K_{gc}U_{hc}+\frac{1}{2}K_{gs}U_{hs}\right]\cos\left(\left|g-h\right|\omega t\right) \\ & +\left[\frac{1}{2}K_{gc}U_{hc}-\frac{1}{2}K_{gs}U_{hs}\right]\cos\left(\left(g+h\right)\omega t\right) \\ & +\left[\frac{1}{2}K_{gc}U_{hs}+\frac{1}{2}K_{gs}U_{hc}\right]\sin\left(\left(g+h\right)\omega t\right) \\ & +\frac{g-h}{\left|g-h\right|}\left[-\frac{1}{2}K_{gc}U_{hs}+\frac{1}{2}K_{gs}U_{hc}\right]\sin\left(\left|g-h\right|\omega t\right) \end{aligned} \tag{6.10}$$

The product is evaluated for all the even harmonic terms in the duty function, $g = 2k-2$ for $k \in [1,2,3,...,N_E]$, and the odd harmonics of interest in the currents and voltages of the converter, $h = 2n-1$ for $n \in [1,2,3,...,N_H]$. Here, N_E is the number of even harmonics, including the constant term, and N_H is the number of odd harmonics considered. The sum of these products in time domain,

$$w\left(t\right) = \sum_{g=0}^{2N_E-2}\sum_{h=1}^{2N_H-1} d\left(g\omega t\right)\cdot u\left(h\omega t\right), \tag{6.11}$$

describe the voltage or current waveform after being processed by the switching cell with duty, $d\left(t\right)$.

In representing the time-domain expression in the frequency-domain, the Fourier coefficients of the input waveform, $u\left(t\right)$, are given by the one-dimensional matrix, U. Similarly, the Fourier coefficients of the output waveform, $w\left(t\right)$, are given by the one-dimensional matrix, W. The square matrix, T, is subsequently derived to map the U-coefficients to the W-coefficients, as follows:

$$W = TU^T \tag{6.12}$$

Both matrices, U and W, have the same form given by Equation (6.4), and describe the input/output voltage or current waveforms before and after being processed by the switching cell in the frequency domain. The actual sine and cosine functions in

$w(t)$ are not included in the T matrix as their coefficients and their position in the matrix can fully describe their specific sinusoidal function and the harmonic number.

The size of the square matrix, T, and the one-dimensional voltage and current matrices are selected as:

$$N_{size} = \begin{cases} 4N_E - 2 & \text{for the buck,} \\ 8N_E - 6 & \text{for the boost and buck-boost,} \end{cases} \tag{6.13}$$

The number of odd harmonics considered in the voltages and currents of the converter is then,

$$N_H = \frac{N_{size}}{2}$$

The T matrix is comprised of four sub-matrices,

$$T = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix}_{2N_H \times 2N_H}, \tag{6.14}$$

where each of the sub-matrices are symmetric around the diagonal. The derivation of the four sub-matrices are exemplified by Figures 6.3-6.6 for up to the eight even harmonic number in the duty function. For each harmonic considered, except for the constant term, a corresponding matrix is added in the derivation of each of the four sub-matrices. The diagonal matrix associated with the constant term, K_0, is added in the derivation of only T_{11} and T_{22}. The matrices are populated with the specified polarity at each position in a diagonally-oriented 'U' pattern, where the vertical spacing between the top and bottom arms is equal to the harmonic number minus one. For example, for the sixth even harmonic terms, the vertical spacing between the two arms is equal to five. All the coefficients, except for the constant term, are divided by two before the matrices are populated.

While only up to the eight even harmonic order is exemplified in the figures, higher terms can be included based on the same developing pattern.

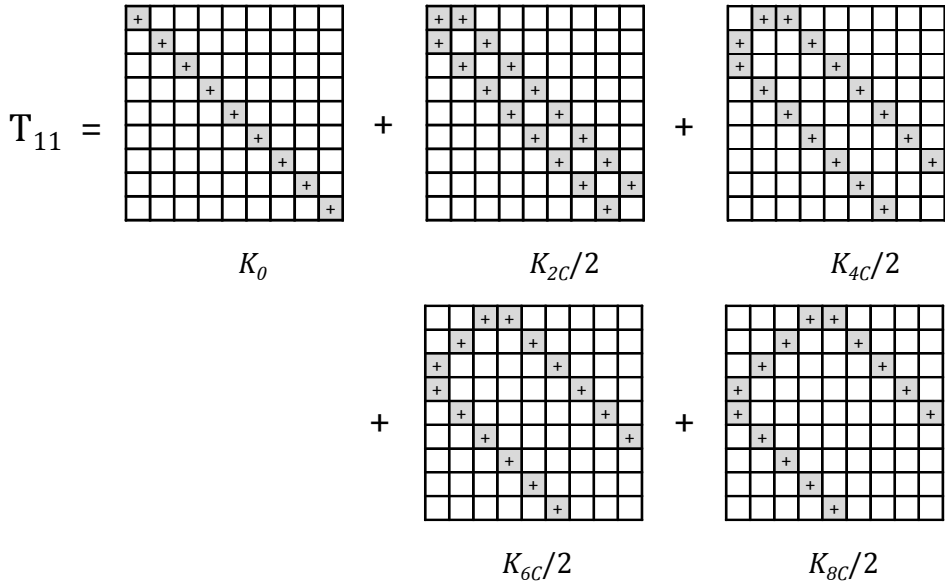


Figure 6.3: The derivation of the sub-matrix T_{11} with up to the eight even harmonic term in the duty-cycle function.

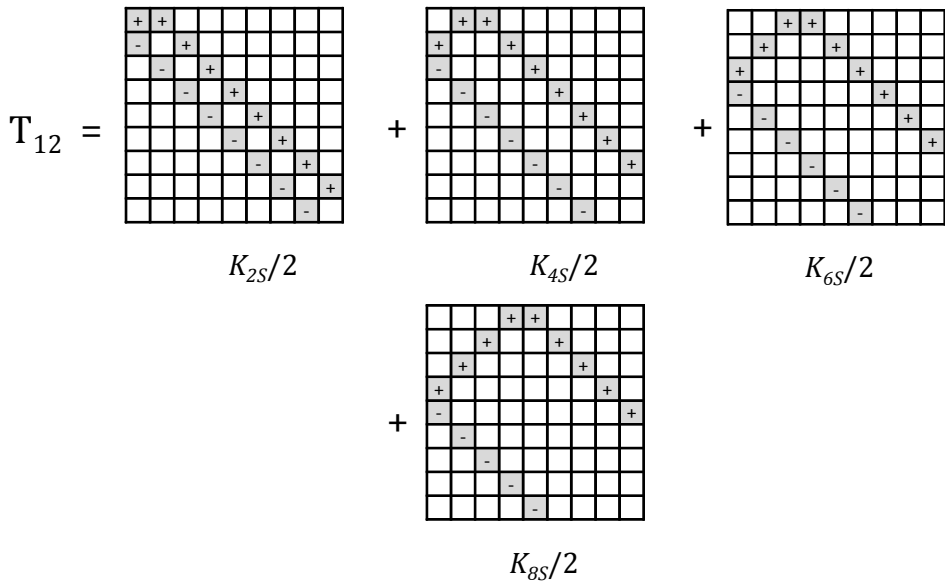


Figure 6.4: The derivation of the sub-matrix T_{12} with up to the eight even harmonic term in the duty-cycle function.

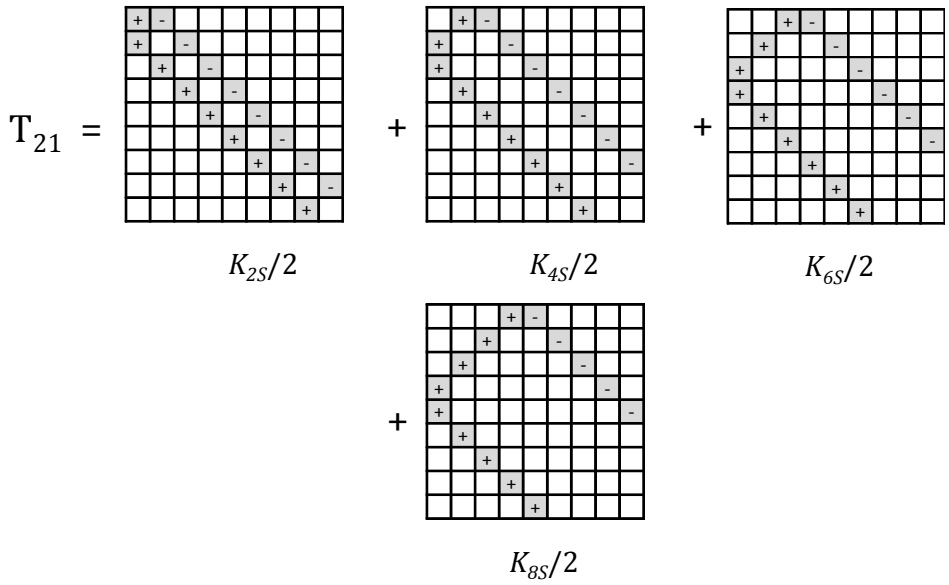


Figure 6.5: The derivation of the sub-matrix T_{21} with up to the eight even harmonic term in the duty-cycle function.

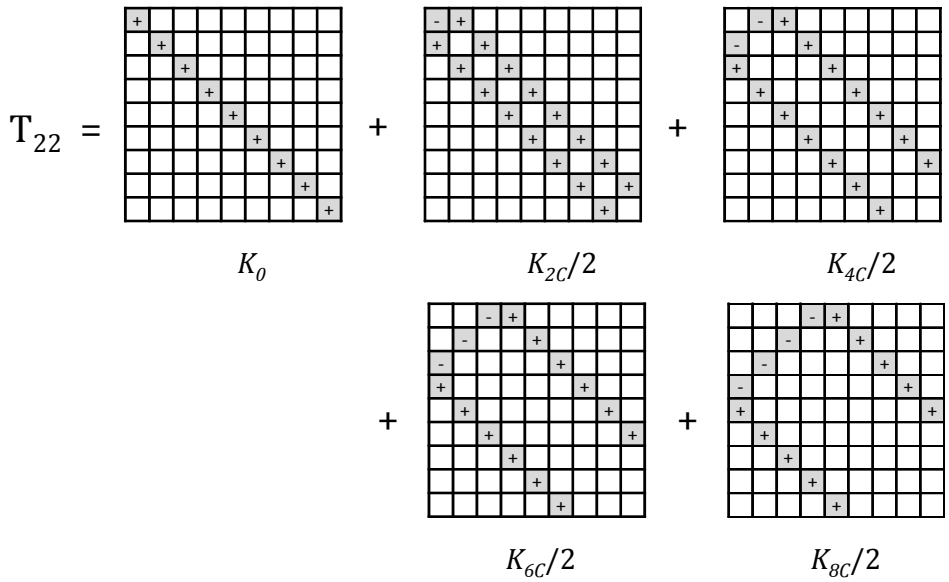


Figure 6.6: The derivation of the sub-matrix T_{22} with up to the eight even harmonic term in the duty-cycle function.

When the duty function, $d(t)$, is utilized as in the case of the buck and the buck-boost, the matrix T is labeled as T_1. When the complement of the duty function, $1-d(t)$, is needed as in the case for the buck-boost and the boost, then the T matrix is derived accordingly and is labeled T_2. The primary differences between the derivation of T_1 based on $d(t)$ and derivation of T_2 based on $1-d(t)$ is that the constant duty term, K_0, is complemented, while the even harmonic terms are negated:

$$1-d(t) = (1-K_0) - K_{2c}\cos(2\omega t) - K_{2s}\sin(2\omega t) \\ - K_{4c}\cos(4\omega t) - K_{4s}\sin(4\omega t) + ...$$

As an example, if the duty function is selected with up to second even harmonic term, $d(t) = K_0 + K_{2c}\cos(2\omega t) + K_{2s}\sin(2\omega t)$, the resulting T_1 matrix for the buck topology is derived as:

$$T_1 = \begin{bmatrix} K_0 + K_{2c}/2 & K_{2c}/2 & 0 & K_{2s}/2 & K_{2s}/2 & 0 \\ K_{2c}/2 & K_0 & K_{2c}/2 & -K_{2c}/2 & 0 & K_{2c}/2 \\ 0 & K_{2c}/2 & K_0 & 0 & -K_{2c}/2 & 0 \\ K_{2c}/2 & -K_{2c}/2 & 0 & K_0 - K_{2c}/2 & K_{2c}/2 & 0 \\ K_{2c}/2 & 0 & -K_{2c}/2 & K_{2c}/2 & K_0 & K_{2c}/2 \\ 0 & K_{2c}/2 & 0 & 0 & K_{2c}/2 & K_0 \end{bmatrix} \tag{6.15}$$

6.5 Derivation of the Injected Current

In solving for the injected current, I_S, for the three configurations of the D-CAP, viz. the buck, the boost or the buck-boost, the following equations are evaluated:

$$I_S^T = \begin{cases} T_1 Y_{RLC} T_1 V_S^T & \text{for the buck,} \\ \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} V_S^T & \text{for the boost,} \\ T_1 \left(I + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} T_1 V_S^T & \text{for the buck-boost,} \end{cases} \tag{6.16}$$

where T_1 is the model of the switching cell based on duty function, $d(t)$; T_2 is the model of the switching cell based on complement of the duty function, $1-d(t)$; Y_{RLC} is the admittance model of the series-connected RLC components in the buck; Z_C is the impedance model of the capacitor, C, in the boost and buck-boost; and Y_{RL} is the admittance model of the series RL components in the boost and buck-boost.

An important feature of this approach is that the models are topology agnostic; whether the topology is a Dynamic Capacitor, Dynamic Inductor or Dynamic Resistor, it does not matter, as the matrices, Y and Z, fully model the characteristics of the network of passive components in the frequency domain.

6.6 Model Validation with Specific Examples

The frequency models are validated using an example case scenario where component values and operating conditions are summarized by Table 6.1.

Table 6.1: The component values and the operating conditions selected in validation of the frequency-domain models.

Operating Condition / Component	Value	Unit	Description
V_S	$480\sqrt{\frac{2}{3}}\sin(\omega t)$	V	Source voltage
C	1	mF	Main capacitor
L	100	μH	Switching inductor
R	0.1	Ω	Parasitic resistance

The duty functions for the three configurations are selected as follows:

$$d(t) = \begin{cases} 0.5 + 0.2\cos(2\omega t) + 0.1\sin(4\omega t) & \text{for the buck,} \\ 0.2 + 0.1\cos(2\omega t) + 0.05\sin(4\omega t) & \text{for the boost,} \\ 0.4 + 0.1\cos(2\omega t) + 0.05\sin(4\omega t) & \text{for the buck-boost.} \end{cases} \tag{6.17}$$

The subsequent size of the T matrices for $G = 4$ are:

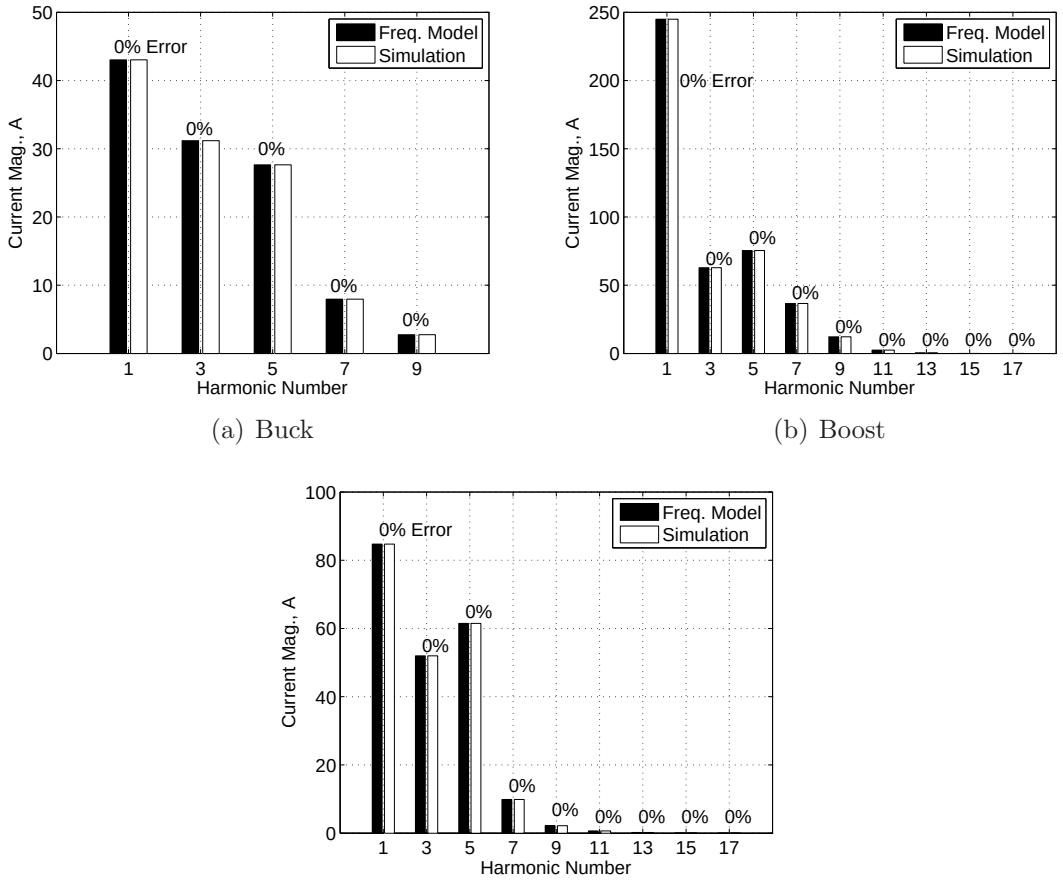
$$N_{size} = \begin{cases} 10 & \text{for the buck,} \\ 18 & \text{for the boost,} \\ 18 & \text{for the buck-boost.} \end{cases} \tag{6.18}$$

For example, the relevant matrices, namely T_1 and Y_{RLC}, for the buck D-CAP are derived as:

$$T_1 = \begin{bmatrix} 0.6 & 0.1 & 0 & 0 & 0 & 0 & 0.05 & 0.05 & 0 & 0 \\ 0.1 & 0.5 & 0.1 & 0 & 0 & 0.05 & 0 & 0 & 0.05 & 0 \\ 0 & 0.1 & 0.5 & 0.1 & 0 & -0.05 & 0 & 0 & 0 & 0.05 \\ 0 & 0 & 0.1 & 0.5 & 0.1 & 0 & -0.05 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0.1 & 0.5 & 0 & 0 & -0.05 & 0 & 0 \\ 0 & 0.05 & -0.05 & 0 & 0 & 0.4 & 0.1 & 0 & 0 & 0 \\ 0.05 & 0 & 0 & -0.05 & 0 & 0.1 & 0.5 & 0.1 & 0 & 0 \\ 0.05 & 0 & 0 & 0 & -0.05 & 0 & 0.1 & 0.5 & 0.1 & 0 \\ 0 & 0.05 & 0 & 0 & 0 & 0 & 0 & 0.1 & 0.5 & 0.1 \\ 0 & 0 & 0.05 & 0 & 0 & 0 & 0 & 0 & 0.1 & 0.5 \end{bmatrix}$$

$$Y_{RLC} = \begin{bmatrix} 0.015 & 0 & 0 & 0 & 0 & 0.38 & 0 & 0 & 0 & 0 \\ 0 & 0.17 & 0 & 0 & 0 & 0 & 1.3 & 0 & 0 & 0 \\ 0 & 0 & 0.79 & 0 & 0 & 0 & 0 & 2.7 & 0 & 0 \\ 0 & 0 & 0 & 4.3 & 0 & 0 & 0 & 0 & 5.0 & 0 \\ 0 & 0 & 0 & 0 & 8.3 & 0 & 0 & 0 & 0 & -3.7 \\ -0.38 & 0 & 0 & 0 & 0 & 0.015 & 0 & 0 & 0 & 0 \\ 0 & -1.3 & 0 & 0 & 0 & 0 & 0.17 & 0 & 0 & 0 \\ 0 & 0 & -2.7 & 0 & 0 & 0 & 0 & 0.79 & 0 & 0 \\ 0 & 0 & 0 & -5.0 & 0 & 0 & 0 & 0 & 4.3 & 0 \\ 0 & 0 & 0 & 0 & 3.72 & 0 & 0 & 0 & 0 & 8.3 \end{bmatrix}$$

The harmonic components of the source current, I_S, are solved using the expressions given by Equation (6.16). The results are compared with the simulations of the average models. The comparison of harmonics is based on their magnitude, $I_h = \sqrt{I_{hc}^2 + I_{hs}^2}$. The comparisons are given by Figure 6.7 for the buck, boost, and buck-boost D-CAP, where there are no observable errors for up to four significant digits; thus, validating the high accuracy associated with the presented modeling approach.



(a) Buck

(b) Boost

(c) Buck-Boost

Figure 6.7: The comparisons of the harmonics in the injected currents obtained from the frequency-domain models and the simulated average models of the D-CAP.

6.7 Accounting for the Input Filter

The input filters that are an integral part of the DVHC implementation for suppressing the switching harmonics have not been considered in the derivation of the frequency models. Their omission has significantly simplified the derivations of the injected current in Equation (6.16). The impact of the input filter is now considered. Example implementations are demonstrated in Figure 6.8 where a third-order filter is utilized at the input of each circuit.

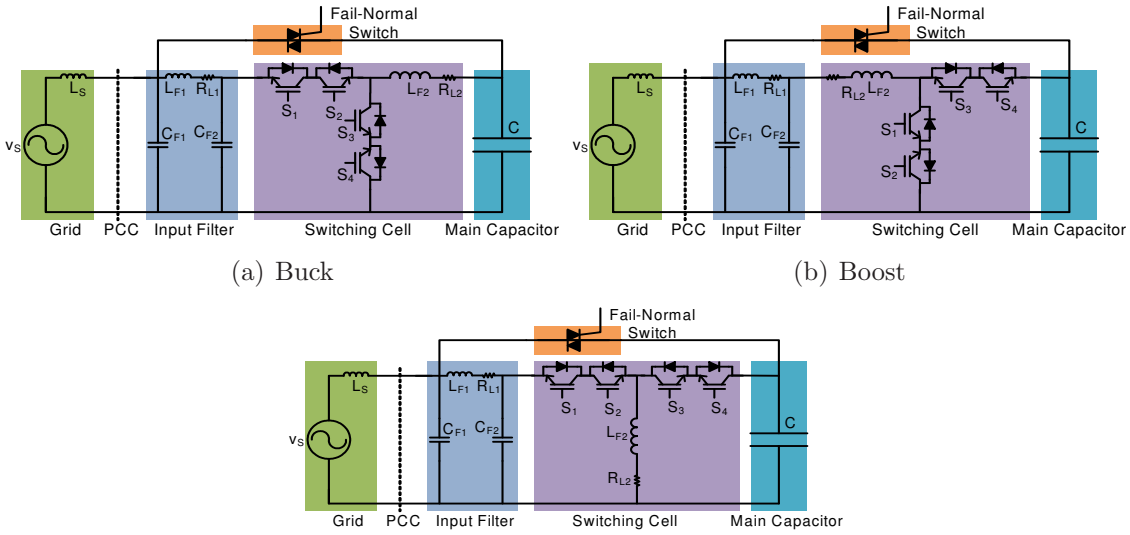


Figure 6.8: The three configurations of the D-CAP.

The passive input filter, regardless of its order, can be represented as a two-port network as exemplified by Figure 6.9.

Figure 6.9: An example two-port network.

The network is described mathematically by,

$$\begin{bmatrix} V_o \\ I_{in} \end{bmatrix}_{4N_H \times 1} = \begin{bmatrix} F_{11} & F_{12} \\ F_{21} & F_{22} \end{bmatrix}_{4N_H \times 4N_H} \begin{bmatrix} V_{in} \\ I_o \end{bmatrix}_{4N_H \times 1}, \tag{6.19}$$

where

$$\begin{aligned} F_{11} &= \left.\frac{V_o}{V_{in}}\right|_{I_o=0}, \\ F_{12} &= \left.-\frac{V_o}{I_o}\right|_{V_{in}=0}, \\ F_{21} &= \left.\frac{I_{in}}{V_{in}}\right|_{I_o=0}, \\ F_{22} &= \left.\frac{I_{in}}{I_o}\right|_{V_{in}=0}. \end{aligned}$$

With the relationship established by Equation (6.19) and the previous current expressions derived in Equation (6.16), a new set of expressions are obtained that include the effect of the input filters:

$$I_S^T = \begin{cases} \left[F_{21} + F_{22}T_1Y_{RLC}T_1\left(\mathrm{I} - F_{12}T_1Y_{RLC}T_1\right)^{-1}F_{11}\right]V_S^T & \text{for the buck,} \\ \left[F_{21} + F_{22}\Theta^{-1}Y_{RL}\left(\mathrm{I} - F_{12}\Theta^{-1}Y_{RL}\right)^{-1}F_{11}\right]V_S^T & \text{for the boost,} \\ \left[F_{21} + F_{22}T_1\Theta^{-1}Y_{RL}T_1\left(\mathrm{I} - F_{12}T_1\Theta^{-1}Y_{RL}T_1\right)^{-1}F_{11}\right]V_S^T & \text{for the buck-boost,} \end{cases} \tag{6.20}$$

where

$$\Theta = \left(\mathrm{I} + Y_{RL}T_2Z_CT_2\right).$$

For the third-order input filters depicted in Figure 6.8, the frequency model is derived at each harmonic number, h, where $h = 2n - 1$ for $n \in [1, 2, 3, ..., N_H]$.

The sub-matrix, F_{11}, is given by,

$$F_{11} = \begin{bmatrix} F_{11}^{11} & F_{11}^{12} \\ F_{11}^{21} & F_{11}^{22} \end{bmatrix}_{2N_H \times 2N_H}, \tag{6.21}$$

where

$$F_{11}^{11}(n,n) = F_{11}^{22}(n,n) = \Re\left(f_{11}(n)\right),$$
$$F_{11}^{12}(n,n) = \Im\left(f_{11}(n)\right),$$
$$F_{11}^{21}(n,n) = -\Im\left(f_{11}(n)\right),$$
$$f_{11}(n) = \frac{1}{1 + \mathrm{j}h\omega R_{L1}C_{F2} - h^2\omega^2 L_{F1}C_{F2}}.$$

The sub-matrix, F_{12}, is given by,

$$F_{12} = \begin{bmatrix} F_{12}^{11} & F_{12}^{12} \\ F_{12}^{21} & F_{12}^{22} \end{bmatrix}_{2N_H \times 2N_H}, \tag{6.22}$$

where

$$F_{12}^{11}(n,n) = F_{12}^{22}(n,n) = \Re\left(f_{12}(n)\right),$$
$$F_{12}^{12}(n,n) = \Im\left(f_{12}(n)\right),$$
$$F_{12}^{21}(n,n) = -\Im\left(f_{12}(n)\right),$$
$$f_{12}(n) = -\frac{R_{L1} + \mathrm{j}h\omega L_{F1}}{1 + \mathrm{j}h\omega R_{L1}C_{F2} - h^2\omega^2 L_{F1}C_{F2}}.$$

The sub-matrix, F_{21}, is given by,

$$F_{21} = \begin{bmatrix} F_{21}^{11} & F_{21}^{12} \\ F_{21}^{21} & F_{21}^{22} \end{bmatrix}_{2N_H \times 2N_H}, \tag{6.23}$$

where

$$F_{21}^{11}(n,n) = F_{21}^{22}(n,n) = \Re\left(f_{21}(n)\right),$$
$$F_{21}^{12}(n,n) = \Im\left(f_{21}(n)\right),$$
$$F_{21}^{21}(n,n) = -\Im\left(f_{21}(n)\right),$$
$$f_{21}(n) = \mathrm{j}h\omega C_{F2}\frac{1 + \frac{C_1}{C_2} + \mathrm{j}h\omega R_{L1}C_{F1} - h^2\omega^2 L_{F1}(h)\, C_{F1}}{1 + \mathrm{j}h\omega R_{L1}C_{F2} - h^2\omega^2 L_{F1}C_{F2}}.$$

And the sub-matrix, F_{22}, is given by,

$$F_{22} = \begin{bmatrix} F_{22}^{11} & F_{22}^{12} \\ F_{22}^{21} & F_{22}^{22} \end{bmatrix}_{2N_H \times 2N_H}, \tag{6.24}$$

where

$$\begin{aligned} F_{22}^{11}(n,n) &= F_{22}^{22}(n,n) = \Re\left(f_{22}(n)\right), \\ F_{22}^{12}(n,n) &= \Im\left(f_{22}(n)\right), \\ F_{22}^{21}(n,n) &= -\Im\left(f_{22}(n)\right), \\ f_{22}(n) &= \frac{1}{1 + \mathrm{j}h\omega R_{L1}C_{F2} - h^2\omega^2 L_{F1}C_{F2}}. \end{aligned}$$

6.8 Inverse Calculation of the Duty Coefficients

The frequency model can be used to numerically back-calculate the coefficients of the duty function that generates a reference source current, I_S^*, with a specific set of harmonics. The formulation of the non-linear constrained equations for the buck, boost and buck-boost D-CAP are:

$$G = \begin{cases} T_1 Y_{RLC} T_1 V_S^T - I_S^{*T} = 0 & \text{for the buck,} \\ \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} V_S^T - I_S^{*T} = 0 & \text{for the boost,} \\ T_1 \left(I + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} T_1 V_S^T - I_S^{*T} = 0 & \text{for the buck-boost.} \end{cases} \tag{6.25}$$

The roots that make each expression equal to zero form a solution-set of optimal duty coefficients for generating the desired reference current. However, the results should be evaluated carefully as the solution-set may not be unique.

The Newton/Raphson method, a gradient-based numerical algorithm, is selected to converge upon the optimal duty coefficients. The general form of the Newton/Raphson algorithm is given by,

$$x^{v+1} = x^v - J^{-1}\left(x^v\right) g\left(x^v\right). \tag{6.26}$$

In obtaining the solutions to a set of nonlinear equations such that $g(x) = 0$, the following steps are taken:

1. Make an initial guess of $x : x^0$. Here let $v = 0$.

2. Calculate $g(x^v)$. If $\|g(x^v)\| \leq \epsilon$, where ϵ is the error tolerance, then x^v is taken as the solution, in which case, terminate the algorithm. Otherwise, go to the next step.

3. Calculate the Jacobian matrix $J(x^v)$.

4. Then calculate $x^{v+1} = x^v - J^{-1}(x^v)\, g(x^v)$. Let $v = v + 1$, and repeat step 2.

In applying the Newton/Rapshon method, the roots take on the following form:

$$x = [K_0\ K_{2c}\ K_{2s}\ K_{4c}\ K_{4s}\ \cdots\ K_{Hc}\ K_{Hs}], \tag{6.27}$$

where

$$\|x\| = K_0 + \sqrt{K_{2c}^2 + K_{2s}^2} + \sqrt{K_{4c}^2 + K_{4s}^2} + \cdots + \sqrt{K_{Nc}^2 + K_{Ns}^2} \leq 1.$$

A duty function with N_M number of coefficients can only control N_M number of harmonic coefficients in the source current, I_S. For the D-CAP, the constant term, K_0, is used to affect the fundamental cosine term of the source current, I_S, providing leading VARs under the assumption that the fundamental of the line voltage is modeled as a sine. The coefficients $K_{(n-1)c}$ and $K_{(n-1)s}$ are used to affect the n-th odd harmonic sine/cosine terms in the source current, I_S. Thus, the matrices in Equation (6.25) are resized to have the same dimension as the number of duty coefficients.

The Jacobian of the non-linear function, G, are calculated as:

$$J = \left[\frac{dG}{dx_1}\ \frac{dG}{dx_2}\ \cdots\ \frac{dG}{dx_i}\ \cdots\ \frac{dG}{dx_{N_M}}\right], \tag{6.28}$$

where

$$\frac{dG}{dx_i} = \begin{cases} \frac{T_1}{dx_i} Y_{RLC} T_1 V_S^T + T_1 Y_{RLC} \frac{T_1}{dx_i} V_S^T & \text{for the buck,} \\ -\left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} \times & \\ \quad \times \left(Y_{RL} \frac{dT_2}{dx_i} Z_C T_2 + Y_{RL} T_2 Z_C \frac{dT_2}{dx_i} \right) \times & \\ \quad \times \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} V_S^T & \text{for the boost,} \\ \frac{dT_1}{dx_i} \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} T_1 V_S^T & \\ \quad -T_1 \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} \times & \\ \quad \times \left(Y_{RL} \frac{dT_2}{dx_i} Z_C T_2 + Y_{RL} T_2 Z_C \frac{dT_2}{dx_i} \right) \times & \\ \quad \times \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} T_1 V_S^T & \\ \quad +T_1 \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} \frac{dT_1}{dx_i} V_S^T & \text{for the boost.} \end{cases}$$

Since the matrices, T_1 and T_2, modeling the behavior of the switching cell are comprised of linear sum of duty coefficients, their derivatives are matrices with constant terms. Thus, these derivatives are pre-calculated when evaluating the Jacobian.

The optimal convergence is evaluated based on least-squares as defined by:

$$\|G\| = \sqrt{|G(1)|^2 + |G(2)|^2 + ... + |G(N_M)|^2} \leq \epsilon. \tag{6.29}$$

6.8.1 Validation of the Numerical Method

The numerical approach to back-calculate the duty coefficients for the three configurations of the D-CAP is validated with examples. It is assumed that the duty function is comprised of up to fourth even harmonic term such that there are five roots:

$$x = [K_0 \;\; K_{2c} \;\; K_{2s} \;\; K_{4c} \;\; K_{4s}]$$

The five roots are only able to affect five harmonic coefficients in the source current. The coefficients are selected as follows:

1. Cosine coefficient of the fundamental frequency.

2. Cosine and sine coefficient of the third harmonic frequency.

3. Cosine and sine coefficient of the fifth harmonic frequency.

The coefficients of the current harmonics are organized in the form,

$$I_S^* = \left\{ \left[\overbrace{\omega \quad 3\omega \quad 5\omega}^{\cos} \qquad \overbrace{3\omega \quad 5\omega}^{\sin} \right] \right.,$$

and are selected as follows for each of the three D-CAP configurations:

$$I_S^* = \begin{cases} [42.95 \;\; 31.17 \;\; -2.51 \;\; -0.75 \;\; 27.53] & \text{for the buck,} \\ [244.2 \;\; 61.76 \;\; -37.50 \;\; 11.75 \;\; 65.45] & \text{for the boost,} \\ [82.65 \;\; 49.80 \;\; -56.87 \;\; 14.94 \;\; 23.40] & \text{for the buck-boost.} \end{cases}$$

These are the same current harmonics generated in the results given by the graphs of Figure 6.7. Therefore, it follows that for the same operating conditions summarized by Table 6.1, the solutions to the non-linear equations should lead to the same original set of duty coefficients.

Tables 6.2-6.4 show the iterations of the Newton/Rapshon algorithm in search of the optimal duty coefficients for the buck, boost and buck-boost D-CAPs, respectively. The data in the tables demonstrate that the coefficients are back-calculated precisely with a small number of iterations.

Table 6.2: Iterations of the Newton/Rapshon algorithm to solve for the duty coefficients in the buck D-CAP.

Iteration #	x^v	$\|G(x^v)\|$
1	[0.6000 0.1000 0.1000 0.1000 0.1000]	42.75
2	[0.5275 0.1730 0.0026 0.0171 0.0841]	6.29
3	[0.5028 0.1964 0.0010 0.0017 0.0979]	0.64
4	[0.5001 0.1999 0.0000 0.0000 0.1000]	0.01
5	[0.5000 0.2000 0.0000 0.0000 0.1000]	$4.03e^{-6}$

The biggest limitations of the Newton/Rapshon algorithm lies in the fact that the initial "guess" of the roots have to be relatively close to the actual roots. The 'wrong' initial guess of the roots can lead to either the wrong set of solutions, as there may be multiple solution sets, or for the algorithm to reach a "run-away" state as the

Table 6.3: Iterations of the Newton/Rapshon algorithm to solve for the duty coefficients in the boost D-CAP.

Iteration #	x^v	$\|G(x^v)\|$
1	[0.5000 0.0000 0.0000 0.0000 0.0000]	379.7
2	[0.3510 0.0206 -0.0151 0.0173 -0.0026]	139.0
3	[0.2451 0.0645 -0.0089 0.0234 0.0268]	49.48
4	[0.2057 0.0931 -0.0001 0.0068 0.0470]	9.868
5	[0.2002 0.0997 0.0000 0.0002 0.0499]	0.3430
6	[0.2000 0.1000 0.0000 0.0000 0.0500]	$4.184e^{-4}$

Jacobian converges to zero. Both of these cases are demonstrated by Tables 6.5 and 6.6 for the case where the algorithm converges to the wrong set of solutions and for the case where the Jacobian converges to zero, respectively. There are modifications that can be applied to the algorithm to not only prevent the run-away conditions but also to ensure that correct and accurate convergence occurs. However, the fact remains that the closer the initial guess is to the actual roots, the faster the Newton/Rapshon algorithm is able to converge upon the correct solution set.

Table 6.4: Iterations of the Newton/Rapshon algorithm to solve for the duty coefficients in the buck-boost D-CAP.

Iteration #	x^v	$\|G(x^v)\|$
1	[0.6000 0.0000 0.0000 0.0000 0.0000]	271.5
2	[0.5072 0.0239 -0.0090 0.0269 0.0087]	88.18
3	[0.4440 0.0536 -0.0058 0.0269 0.0293]	29.63
4	[0.4134 0.0812 -0.0013 0.0132 0.0431]	9.640
5	[0.4025 0.0962 -0.0000 0.0029 0.0484]	1.784
6	[0.4001 0.0998 0.0000 0.0002 0.0499]	$9.626e^{-2}$
7	[0.4000 0.1000 0.0000 0.0000 0.0500]	$3.603e^{-4}$

Table 6.5: The Newton/Rapshon algorithm wrongly solves for the duty coefficients in the boost D-CAP.

Iteration #	x^v	$\|G(x^v)\|$
1	[0.9 0.0000 0.0000 0.0000 0.0000]	683.8
2	[0.8662 0.0000 0.0168 -0.0156 -0.0200]	140.2
3	[0.8713 -0.0031 0.0139 -0.0107 -0.0167]	2.525
4	[0.8713 -0.0035 0.0141 -0.0104 -0.0171]	$5.6e^{-3}$

Table 6.6: The Newton/Rapshon algorithm goes out of bounds when searching for the duty coefficients of the boost D-CAP.

Iteration #	x^v	$\|G(x^v)\|$
1	[0.8 0.0000 0.0000 0.0000 0.0000]	1585
2	[0.9541 -0.0138 0.0011 0.0012 -0.0142]	1390
3	[0.7613 0.0702 0.0117 -0.0449 0.0472]	1.37
4	[0.1210 -0.0140 0.6179 -0.3237 -0.0278]	1237
5	[0.7600 5.068 0.3653 -0.9289 -2.178]	757.3
8	$[-5.829e^5\ -1.167e^6\ 3.547e^5\ -8.211e^5\ 3.250e^5]$	263.2
11	$[-3.204e^{145}\ 6.223e^{145}\ 2.419e^{144}\ -3.292e^{145}\ 1.299e^{145}]$	263.2
12	[NaN NaN NaN NaN NaN]	NaN

6.9 Conclusions

Frequency-domain models that are able to accurately describe the steady-state harmonic behavior of the D-CAP are presented in this chapter. The models are derived from the single-phase average models in the stationary reference frame. For a source voltage with harmonic components, and for a duty function with a certain set of coefficients under EHM operation, the models are able to accurately predict the harmonic coefficients of any voltage or current in the circuit. Furthermore, through numerical techniques, the duty coefficients can in turn be inversely calculated for a given set of harmonic coefficients in the currents or voltages. Thus, this becomes an extremely powerful tool for analyzing the operation of the DVHCs, especially since there is bound to be some level of harmonics on the grid; even for purely VAR compensation applications.

The frequency-domain models can be mapped to the time domain through Fourier series representation where the coefficients of voltage or current at particular harmonics become the Fourier coefficients, a_h and b_h, in the following expression:

$$f(\omega t) = \sum_{h=1}^{N_H} [a_h \cos(h\omega t) + b_h \sin(h\omega t)],$$

where a_h are the coefficients of the sine terms and b_h are the coefficients of the cosine terms for the harmonic number, h.

CHAPTER VII

CONTROL WITH HIGH SWITCHING FREQUENCY

7.1 Introduction

Although the DVHCs have simple power architectures comprised of a single-phase direct AC converter interfaced to a passive component, their operation with EHM is quite complex because the relationship between control handles and the corresponding controlled variables is not very well understood.

The frequency-domain models of the buck, boost and buck-boost configurations of the D-CAP are used to perform a sensitivity analysis to establish the relationship between the odd harmonics in the injected current and the even harmonic terms in the duty function when the converter is operated under a high-frequency-synthesis assumption. The type of sensitivity analysis selected is based on localized methods where a simple derivative of the output current is taken with respect to the variables in the duty function and evaluated for a set of the duty values.

Based on the results of the sensitivity analysis, single- and three-phase control architectures with linear controllers in the synchronous reference frame are presented for controlling the D-CAP. A heuristic approach to tuning the control gains is discussed. The effectiveness of the control architectures are validated through simulation.

The stability margins under closed-loop control are assessed for different gain values of the compensator that is controlling the supply of reactive power. The stability is evaluated using the transfer functions derived from the small-signal models.

The focus of this chapter is on the D-CAP, but the discussions and approaches can be extended to the D-IND and D-RES with minimal effort.

7.2 Sensitivity Analysis Using Localized Methods

Using the frequency-domain model established in Chapter 6, the harmonic coefficients of the injected currents for the three configurations of the D-CAP are calculated as:

$$I_S^T = \begin{cases} T_1 Y_{RLC} T_1 V_S^T & \text{for the buck,} \\ \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} V_S^T & \text{for the boost,} \\ T_1 \left(I + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} T_1 V_S^T & \text{for the buck-boost,} \end{cases} \tag{7.1}$$

where T_1 is the model of the switching cell based on duty function, $d\,(t)$; T_2 is the model of the switching cell based on complement of the duty function, $1 - d\,(t)$; Y_{RLC} is the admittance model of the series-connected RLC components in the buck; Z_C is the impedance model of the capacitor, C, in the boost and buck-boost; and Y_{RL} is the admittance model of the series RL components in the boost and buck-boost.

The matrices modeling the behavior of the switching cells, T_1 and T_2, contain the duty coefficients that induce the desired harmonics in the current, I_S. Organized by their corresponding harmonic number, the duty coefficients are:

$$d = \begin{bmatrix} K_0 & K_{2C} & K_{2S} & K_{4C} & K_{4S} & K_{6C} & K_{6S} & \cdots \end{bmatrix}$$

where the numerical subscript denotes the harmonic number the coefficient is associated with, while the letter subscripts, C and S, denote cosine and sine terms, respectively.

To understand which coefficient should be used to control a specific harmonic number, a sensitivity analysis is undertaken. It is well understood from the previous chapters that the constant term, K_0, is used to control the leading VARs at the fundamental frequency. The sensitivity analysis will establish a similar correlation between a given even harmonic duty coefficient and the corresponding odd harmonic in the injected current.

To begin the analysis, the derivatives of the expressions in Equation (7.1) are taken with respect to each of the six even harmonic duty coefficients. If a definitive

relationship can be established up to the sixth harmonic terms, the same pattern can be assumed to exist for the higher order harmonics as well.

The derivatives, with respect to each even harmonic coefficient in the duty function, are:

$$\frac{d}{dK_\Psi} I_S^T = \begin{cases} \frac{T_1}{dK_\Psi} Y_{RLC} T_1 V_S^T + T_1 Y_{RLC} \frac{T_1}{dK_\Psi} V_S^T & \text{for the buck,} \\ -\left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} \times & \\ \quad \times \left(Y_{RL} \frac{dT_2}{dK_\Psi} Z_C T_2 + Y_{RL} T_2 Z_C \frac{dT_2}{dK_\Psi} \right) \times & \\ \quad \times \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} V_S^T & \text{for the boost,} \\ \frac{dT_1}{dK_\Psi} \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} T_1 V_S^T & \\ \quad -T_1 \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} \times & \\ \quad \times \left(Y_{RL} \frac{dT_2}{dK_\Psi} Z_C T_2 + Y_{RL} T_2 Z_C \frac{dT_2}{dK_\Psi} \right) \times & \\ \quad \times \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} T_1 V_S^T & \\ \quad +T_1 \left(\mathrm{I} + Y_{RL} T_2 Z_C T_2\right)^{-1} Y_{RL} \frac{dT_1}{dK_\Psi} V_S^T & \text{for the buck-boost,} \end{cases} \tag{7.2}$$

where

$$\Psi = [2C, 2S, 4C, 4S, 6C, 6S].$$

The duty cycle is inherently restricted within the range, $d(t) \in [0, 1]$, as the duty of a switch cannot be above 100 percent and nor can it be negative. The constant term, K_0, is selected based on nominal operating point of the respective configuration. Further, for the boost and buck-boost configuration, component values are appropriately designed to ensure that their natural frequencies, as given by $\omega_0 = \frac{1-K_0}{\sqrt{L_F C}}$, do not coincide with the odd harmonics that need to be compensated.

The even harmonic coefficients are all selected with equal magnitudes in order to mitigate an external bias, while ensuring the norm of the duty coefficients remains

bound within the unit circle as:

$$\|d\| = K_0 + \sqrt{K_{2C}^2 + K_{2S}^2} + \sqrt{K_{4C}^2 + K_{4S}^2} + \sqrt{K_{6C}^2 + K_{6S}^2} \leq 1$$

The derivatives are evaluated under realistic operating conditions with an example design based on the operating conditions, component values, and duty coefficients summarized in Table 7.1 for the buck, boost and buck-boost D-CAP.

Table 7.1: The operating conditions and the component values used in the sensitivity analysis of the D-CAP.

Operating Condition / Component	Value	Unit	Description
V_S	$480\sqrt{\frac{2}{3}}$	V	Source voltage
C	1	mF	Main capacitor
L	100	μH	Switching inductor
R	0.1	Ω	Parasitic resistance
$d\,(h)$	[0.5 0.11 0.11 0.11 0.11 0.11 0.11]	-	Buck duty
	[0.3 0.07 0.07 0.07 0.07 0.07 0.07]	-	Boost duty
	[0.7 0.07 0.07 0.07 0.07 0.07 0.07]	-	Buck-boost duty

The results are normalized by dividing by the reactive current of the main capacitor, C, when it is interfaced directly to the grid:

$$\Gamma = \frac{dI_S}{dK_\Psi} / I_{BASE}, \tag{7.3}$$

where

$$I_{BASE} = V_m \omega C, \tag{7.4}$$

$$\Psi = [2C, 2S, 4C, 4S, 6C, 6S].$$

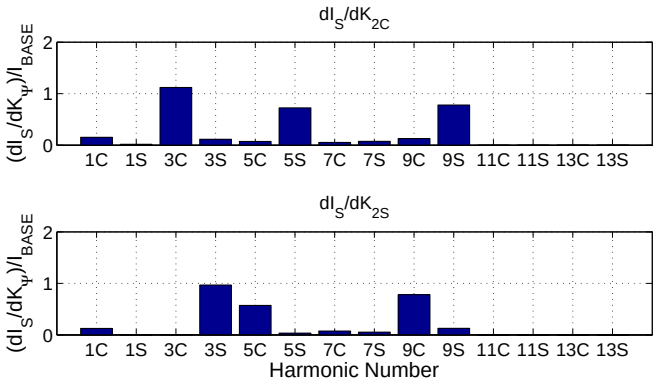
The results of differentiating the current expressions with respect to second, fourth, and sixth harmonics of the duty function are given by Figures 7.1(a), 7.1(b), and 7.1(c), respectively, in the form of bar graphs for the buck configuration. Similarly, Figures 7.2(a)-(c) are the results for the boost, and Figures 7.3(a)-(c) are the results

for the buck-boost. Two bar graphs are shown per sub-figure, where the top graph corresponds to differentiation with respect to the cosine term and the bottom graph with respect to the sine term. The discrete datasets of the 18 bar graphs are identical, where both the sine and cosine terms of the current harmonics for up to the 13th harmonics are plotted.

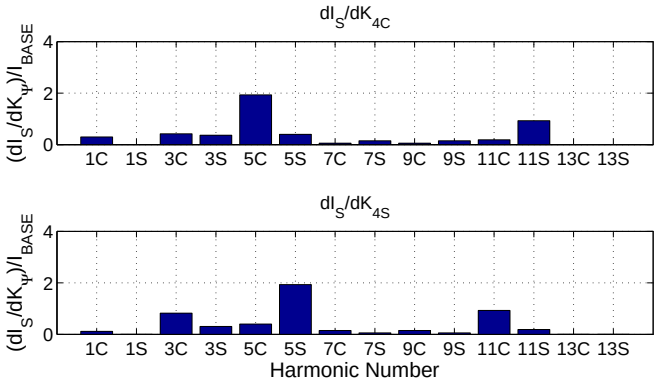
While the boost D-CAP, with up to the sixth even harmonic term in the duty, induces up to the 25th harmonic in the current, and even higher number of harmonics still with the buck-boost, the seven duty coefficients can only control seven harmonic coefficients in the current. Therefore, the whole harmonic spectrum of the D-CAP current is not plotted.

The 18 graphs indicate that the $(n-1)$-th even harmonic term in the duty function has the highest impact on the n-th odd harmonic term in the current. More specifically, the cosine coefficient of the $(n-1)$-th even harmonic term in the duty function has the highest impact on the n-th odd harmonic cosine coefficient of the current. Similarly, the sine component of the duty coefficient has the highest impact on the sine term of the current.

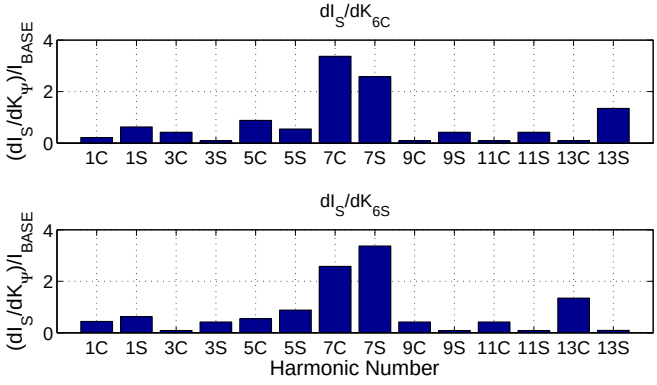
As can be seen from these graphs, there are multiple harmonics that are sensitive to changes to a particular duty coefficient. In other words, multiple harmonics are tightly coupled together, such that changing the coefficient of any one even harmonic term in the duty function can affect multiple odd harmonics in the current. This characteristic poses a very unique control challenge. It is these inter-harmonic couplings, where energy is exchanged between adjacent harmonics that enable a single-phase direct AC converter to provide harmonic filtering in the first place. However, when one control handle influences multiple output variables, controlling any one variable requires juggling multiple handles. One approach to prevent controllers that compensate different harmonics from fighting is to have each adjacent control loops tuned with different time constants, such that each loop is operating at different speeds.



(a) With respect to the second even harmonic

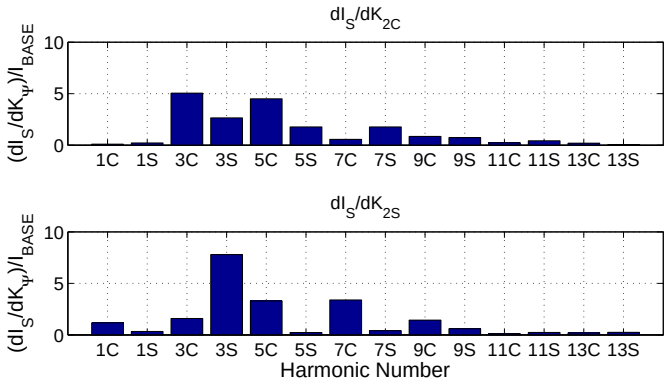


(b) With respect to the fourth even harmonic

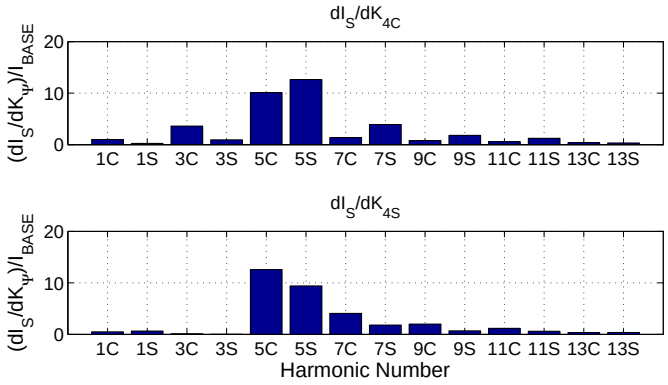


(c) With respect to the sixth even harmonic

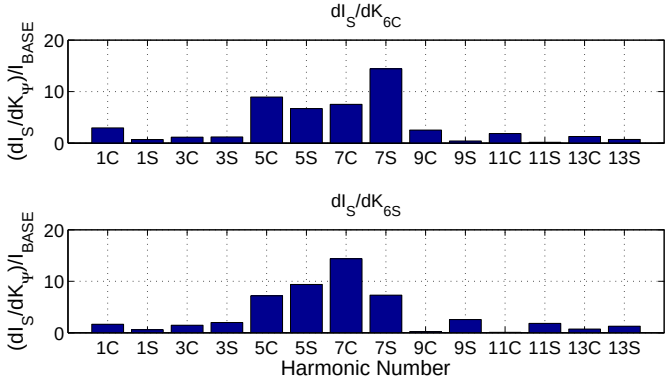
Figure 7.1: The sensitivity of the current harmonics (plotted as the discrete data set along the x-axes) to the six duty coefficients, where the current harmonic with the tallest bar represents the highest sensitivity for the given duty coefficients of the buck D-CAP.



(a) With respect to the second even harmonic

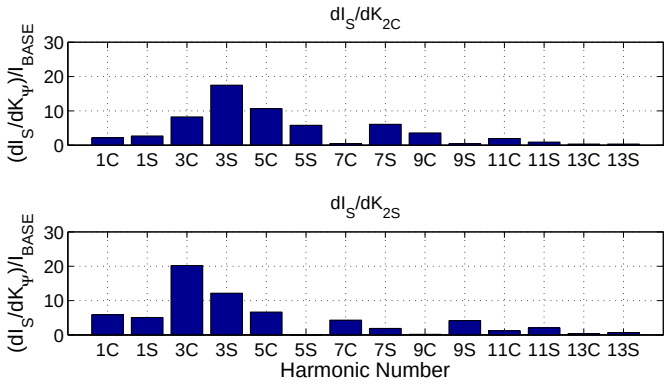


(b) With respect to the fourth even harmonic

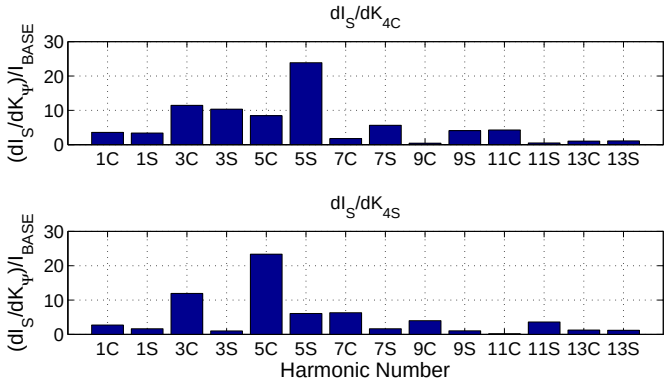


(c) With respect to the sixth even harmonic

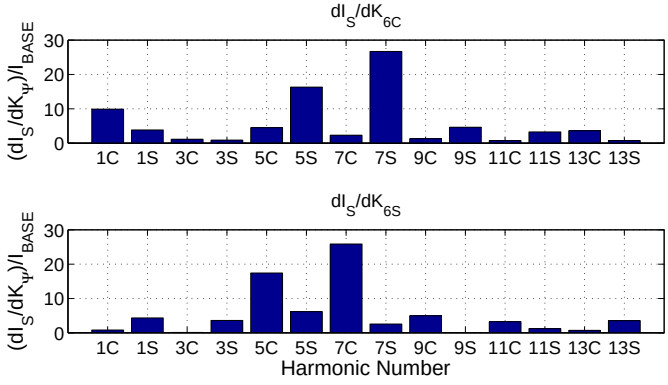
Figure 7.2: The sensitivity of the current harmonics (plotted as the discrete data set along the x-axes) to the six duty coefficients where the current harmonic with the tallest bar represents the highest sensitivity for the given duty coefficients of the boost D-CAP.



(a) With respect to the second even harmonic



(b) With respect to the fourth even harmonic



(c) With respect to the sixth even harmonic

Figure 7.3: The sensitivity of the current harmonics (plotted as the discrete data set along the x-axes) to the six duty coefficients where the current harmonic with the tallest bar represents the highest sensitivity for the given duty coefficients of the buck-boost D-CAP.

The faster loops are able to compensate for undesirable changes made by the slower loops. The loops that are attempting to shuffle the most amount of reactive power are tuned the slowest. Therefore, the fundamental loop is typically tuned the slowest relative to the other loops, while the loop for the highest order harmonic is tuned to be the fastest, as a lesser amount of reactive compensation is required at higher frequencies.

Another characteristic that can be observed from the bar graphs is that the sensitivity level (heights of the bar) increases when differentiating with respect to higher even harmonic term for all three configurations. For example, levels corresponding to differentiation with respect to the sixth even harmonic term in Figure 7.1(c) are generally higher than levels that correspond to differentiation with respect to the fourth even harmonic term in Figure 7.1(b) for the buck. While the levels in Figure 7.1(b) are higher than in Figure 7.1(a), where the latter sub-figure corresponds to differentiation with respect to the second even harmonic term. The same characteristics are manifested in the graphs of Figure 7.2 and Figure 7.3 for the boost and buck-boost, respectively. This is because a capacitor with a voltage, $V_C(t) = \sin(n\omega t)$, will draw a current that is proportional to the frequency of the voltage imposed across it, or $n\omega$. Therefore, it follows that the higher even harmonic terms in the duty cycle induces a current injected by D-CAP of higher magnitude, especially since the duty excitations for all the even harmonic terms are of equal magnitude in this study.

Combining this characteristics of a capacitor with the fact that the current harmonics generated by a non-linear load typically decreases with increasing harmonic number, $|I_{LOAD}(n\omega)| < |I_{LOAD}((n-2)\omega)|$, leads to the conclusion that the control effort required to filter a higher harmonic current is lower than the control effort required to filter a current of lower harmonic number, or $|K_{n-1}| < |K_{n-3}|$.

7.3 Control in the Synchronous Reference Frame

The advantage of designing a control system in the synchronous (or rotating) reference frame is that since the sinusoidal variables of the stationary reference frame have been mapped over as a constant (or DC) in the synchronous reference frame, simple PID-based controllers that have been widely used with DC-DC converters are directly applicable to direct AC converters like the D-CAP. The transformation to provide the mapping from the stationary to the synchronous reference frame, and vice versa, for the various voltages and currents in the system are given by,

$$T_{dq0/abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\omega t) & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) \\ \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}, \tag{5.18}$$

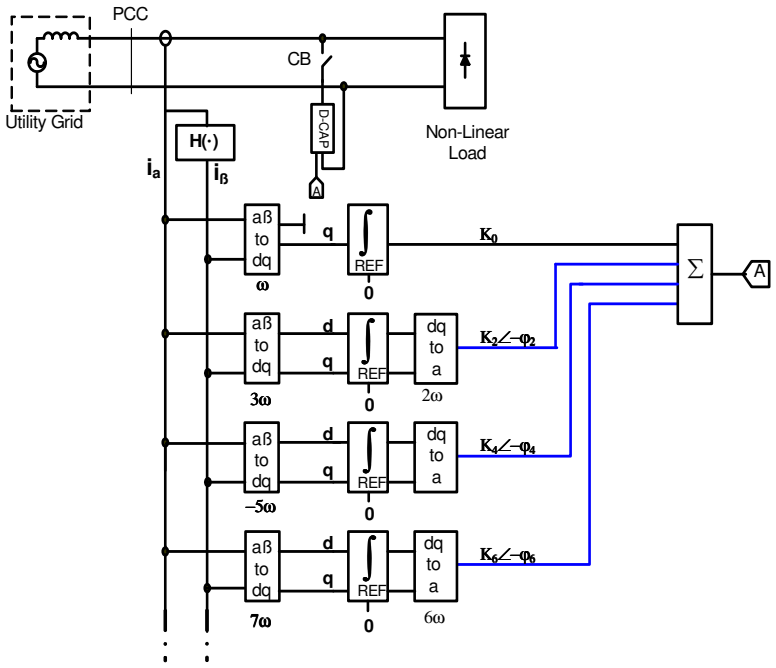
where the transpose of the matrix enables transformation from synchronous back to the stationary reference frame as given by,

$$T_{abc/dq0} = T^{-1}_{dq0/abc} = T^{T}_{dq0/abc}. \tag{7.5}$$

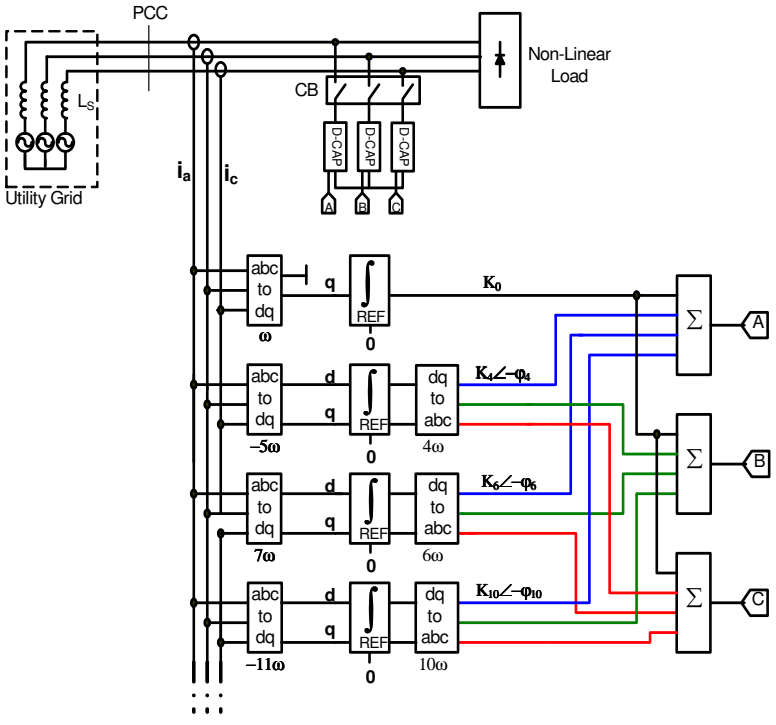
The former transformation is called the ABC-to-DQ0 transformation, as previously defined, and the latter is called the DQ0-to-ABC transformation.

For the D-CAP operating as a harmonic filter that is compensating for multiple harmonics, a control loop at each frequency of interest is designed, including one at the fundamental frequency for power factor correction or voltage support. The single- and three-phase control architectures suitable for controlling the D-CAP are depicted in Figure 7.4.

The single-phase control architecture is applicable for a three-phase system as well, but with each phase independently controlled. For the three-phase control architecture, balanced and symmetrical operation is implied. As this operating state is quite rare, especially with the plethora of single-phase loads on the system, the single-phase control architecture is considered more practical and versatile.



(a) Single-phase



(b) Three-phase

Figure 7.4: Control architectures of the D-CAP in the synchronous reference frame for a single- and three-phase implementations.

In transforming the sinusoidal variables of a single-phase system to the synchronous reference frame, a transformation, $H(\cdot)$, is required to obtain the orthogonal component. The various approaches in deriving this orthogonal component are discussed in [27, 79].

For both single- and three-phase architectures, there are essentially two types of control loops: one for injecting leading VAR at the fundamental frequency, and the rest for harmonic filtering. However, for the loop at the fundamental frequency, there are two potential and very different control objectives:

1. Power factor correction (PFC), especially when interfacing industrial loads, or,

2. Voltage support.

In providing power factor correction, the fundamental component of the line current in each of the phases is made to be in-phase with its corresponding line voltage, thus allowing the power factor to reach unity. If the load is drawing inductive (lagging) current, by injecting the correct amount of capacitive (leading) current, the reactive power requirements of the load can be directly addressed by the D-CAP such that the power grid effectively sees a resistive load. In the synchronous reference frame, this objective is achieved by feeding back the quadrature component of the line current to the controller and driving it to zero. The quadrature component is obtained through the ABC-to-DQ0 transformation with the fundamental frequency, ω, as a reference. This controller is demonstrated in Figure 7.4 and described as follows:

$$K_0 = G_{1q} \int_0^t e_1(\tau)\, d\tau, \tag{7.6}$$

where

$e_1(t) = I_{q1}$,

$I_{q1} \equiv$ quadrature component of the line current at the fundamental frequency,

$G_{1q} \equiv$ gain of the integrator,

$K_0 \equiv$ constant term of the duty function.

Here, only a simple integrator is employed in generating the appropriate duty command. A proportional term can be used as well, but in the presence of the harmonics in the line current, without a low pass filter, the performance would be poor. If a low pass filter is used, the speed or bandwidth of the control loop would slow down. This especially applies to single-phase systems where the low pass filter would have to be designed to suppress a 120 Hz signal in the synchronous reference frame, corresponding to the third harmonic in the stationary reference frame.

The triplen harmonics do not exist on a three-phase, three-wire system, so the first harmonic to be compensated is the 5th. Therefore, the low pass filter can be designed with higher cut-off frequency.

In providing voltage support when there is a fault on the power system or when the system is attempting to recover from a fault, instead of using current as a feedback, the magnitude of the line voltage is used. Without adequate supply of reactive power to compensate for the voltage drop on the lines, the grid voltage tends to droop. As more leading VARs are injected by the D-CAP, the voltage magnitude starts to rise. With a proper level of injection, the voltage magnitude can be controlled to within a certain tolerance band. The voltages in the synchronous reference frame, V_d and V_q, are obtained using the ABC-to-DQ0 transformation with the fundamental frequency, ω, as reference. In implementing this objective, the controller on the fundamental frequency loop of Figure 7.4 is replaced with

$$K_0 = G_{1d} \int_0^t e_1(\tau)\, d\tau, \tag{7.7}$$

where

$$e_1(t) = V_d^* - V_d,$$

$V_d^* \equiv$ reference direct component of the line voltage,

$V_d \equiv$ direct component of the line voltage,

$G_{1d} \equiv$ gain of the integrator,

$K_0 \equiv$ constant term of the duty function.

Here, only the direct component of the voltage, V_d, is required because the PLL synchronizes with the line voltages such that the $V_q = 0$. The output of the integrator is saturable to limit the duty within the valid range, $d(t) \in [0, 1]$.

In filtering the harmonics from the line current, there is a control loop for each harmonic of interest as follows:

$$K_{nd} = G_{nd} \int_0^t e_{nd}(\tau)\, d\tau, \tag{7.8}$$

$$K_{nq} = G_{nq} \int_0^t e_{nq}(\tau)\, d\tau, \tag{7.9}$$

where

$e_{nd}(t) = -I_{nd}$,

$e_{nq}(t) = -I_{nq}$,

$I_{nd} \equiv$ direct component of the line current at the n-th harmonic,

$I_{nq} \equiv$ quadrature component of the line current at the n-th harmonic,

$G_{nd} \equiv$ integrator gain of n-th harmonic's direct component,

$G_{nq} \equiv$ integrator gain of n-th harmonic's quadrature component,

$K_{nd} \equiv$ direct component of the duty coefficient of the n-th harmonic,

$K_{nq} \equiv$ quadrature component of the duty coefficient of the n-th harmonic.

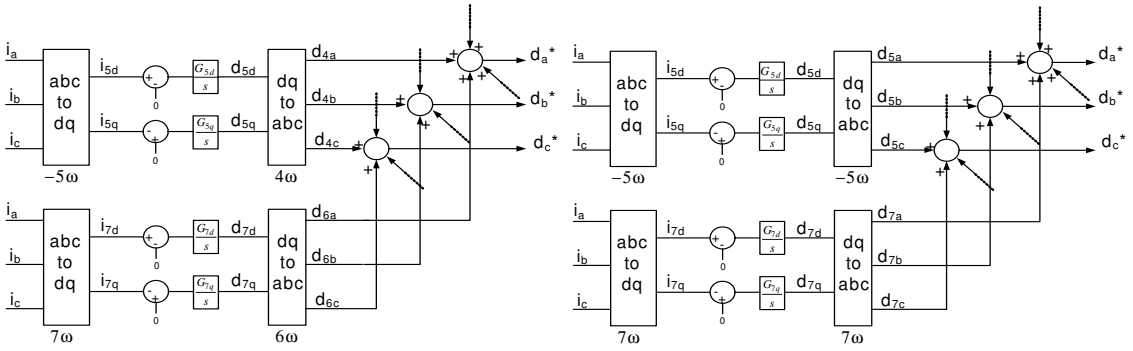
Such a controller is depicted in Figure 7.4. The direct and quadrature components of the line current at the n-th harmonic are obtained using the ABC-to-DQ0 transformation with the harmonic frequency, $n\omega$, as reference. In transforming the duty

commands, K_{nd} and K_{nq}, in the synchronous reference frame back to the stationary reference frame, the DQ0-to-ABC transformation is employed with $(n-1)\,\omega$ as the reference frequency, resulting in

$$\begin{bmatrix} K_{(n-1)a} \\ K_{(n-1)b} \\ K_{(n-1)c} \end{bmatrix} = T^{-1}|_{(N-1)\omega} \begin{bmatrix} K_{nd} \\ K_{nq} \\ 0 \end{bmatrix}. \tag{7.10}$$

The ABC outputs of each of the harmonic control loops are summed together, on a per-phase basis, along with the constant output of the fundamental loop. The summations are applied as the duty cycles to each phase of the D-CAP in the three-phase system. For the single-phase control architecture, there is only one phase.

The control architectures are very similar to that used by inverter-based active filter topologies in Figure 7.5. Due to the similarities, the control resources required, in terms of sensors, signal conditioning circuits, speed and features of the DSP, etc., are comparable.



(a) D-CAP (b) VSI

Figure 7.5: Example harmonic controllers for the D-CAP and the VSI-based active filters.

7.4 Heuristic Tuning of the Controller

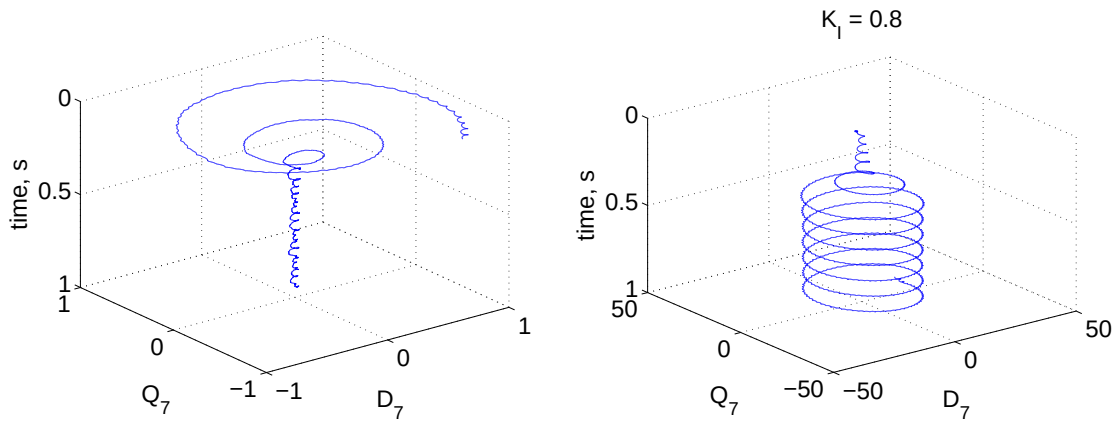
The controller is tuned with a descending harmonic order where the control loop compensating for the highest current harmonic is tuned first, while the fundamental

loop is tuned the last.

While the harmonic control loops are being tuned, the output of the fundamental control loop, K_0, is fixed to a nominal value. The main capacitor, C, is typically sized such that $K_0 = 0.5$ for the buck and buck-boost, and $K_0 = 0.2$ for the boost D-CAP. For the three-phase architecture shown in Figure 4(b), the loop compensating for the 11th harmonic current is tuned first. The D and Q integral gains are incrementally increased together by 10 to 20 percent until either no further improvements in response is obtained, or duty cycle goes out of bounds. When the duty cycle goes out of the bound, the controller becomes unstable. In such a case, the gain values are decreased back by 10 to 20 percent until duty cycle remains bounded.

The loop compensating for the 7th harmonic current is tuned next. Similar steps are taken for tuning this loop as well. To prevent cross-coupling between the loops, the gains are adjusted such that a given harmonic control loop operates at a different speed compared to the adjacent loops. However, in a three-phase, three-wire system, because the triplens do not exist, the 7th harmonic loop is two odd harmonic numbers away from the 11th. Thus, significantly less cross-coupling takes place.

Figure 7.6 shows a pair of three-axis plots of the DQ current error versus time for the 7th harmonic loop for different values of the integral gains. In Figure 7.6(a), with a gain of 0.4, the controller converges to $(D, Q) = (0, 0)$ relatively well behaved. In Figure 7.6(b), the controller is quasi-stable with the gain value of 0.8, as the DQ vector fluctuates around the $(D, Q) = (0, 0)$ point. However, the controller is not able to lock onto the 7th harmonic current generated by the load, and thus is unable to cancel it. This is because the duty cycle generated by the control loop has exceeded the [0,1] range and is unable to converge again. In fact, the control loop is injecting its own share of undesired harmonics into the grid. Thus, to realize the best performance from the controller, the gain should be tuned such that it never encounters the quasi-stability or unstable region.



(a) $G_{Id7} = G_{Iq7} = 0.4$ (b) $G_{Id7} = G_{Iq7} = 0.8$

Figure 7.6: The average D and Q current errors versus time for the 7th harmonic control loop of an arbitrary system for two integral gains where the larger gain leads to quasi-stability.

The loop compensating for the 5th harmonic current is tuned in a similar fashion. However, unlike the 7th harmonic loop, the 5th harmonic loop is only one odd harmonic number away from the 7th, so there is a potential for significant cross-coupling to take place. Thus, the gains of the 5th harmonic loop have to be tuned such that the loop operates either slower or faster than the loop for the 7th harmonic current, depending on which is a more stable operating point.

Once, all the harmonic loops are tuned, the control loop at the fundamental frequency is tuned the last, and tuned to be the slowest. The individual D and Q gains in each of the loop can be tuned to further tweak response and performance. If the gains of the loops are tuned properly, the control loops drive their respective DQ terms to zero in a very well behaved and stable manner as demonstrated in Figure 7.7.

7.5 Simulation of the Three-Phase Control Architecture

Closed-loop operation of the buck D-CAP depicted in Figure 7.8 is demonstrated for the values and operating conditions given by Table 7.2. While the buck D-CAP is

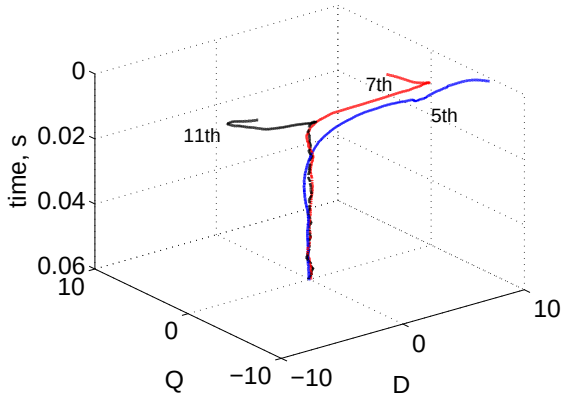


Figure 7.7: A stable and well-behaved convergence of the D and Q component to zero in the 5th, the 7th, and the 11th harmonic control loops.

employed in this demonstration, the same control architectures are also applicable to both the boost and buck-boost D-CAPs as well. The controller gains are summarized by Table 7.3.

Table 7.2: The operating conditions and the component values selected for validating the effectiveness of the D-CAP controllers.

Operating Condition / Component	Value	Unit	Description
V_S	$240\sqrt{\frac{2}{3}}$	V	Source voltage
L_S	200	μH	Source impedance
C	750	μF	Main capacitor
C_{F1}	400	μF	Input filter capacitor 1
C_{F2}	100	μF	Input filter capacitor 2
L_{F1}	20	μH	Input filter inductor
L_{F2}	200	μH	Switching inductor
R	0.1	Ω	Parasitic resistance

The results of the D-CAP operating with nominal grid voltages are shown in Figure 7.9. The line current is not only in phase with the line voltage, but it is also free of all the harmonics up to the 13th harmonic. The harmonic currents injected by the D-CAP are in anti-phase with the harmonic currents generated by the load,

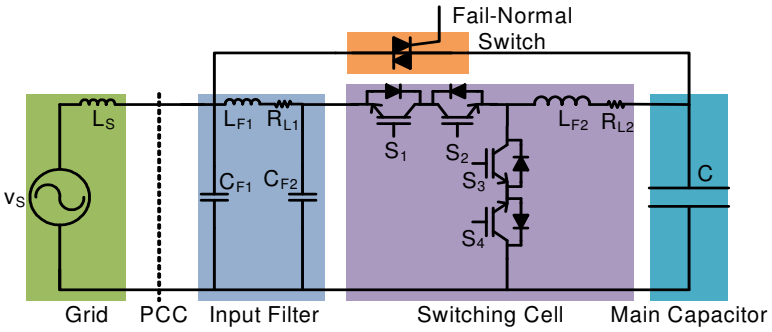


Figure 7.8: The topology of the buck D-CAP considered for the simulation.

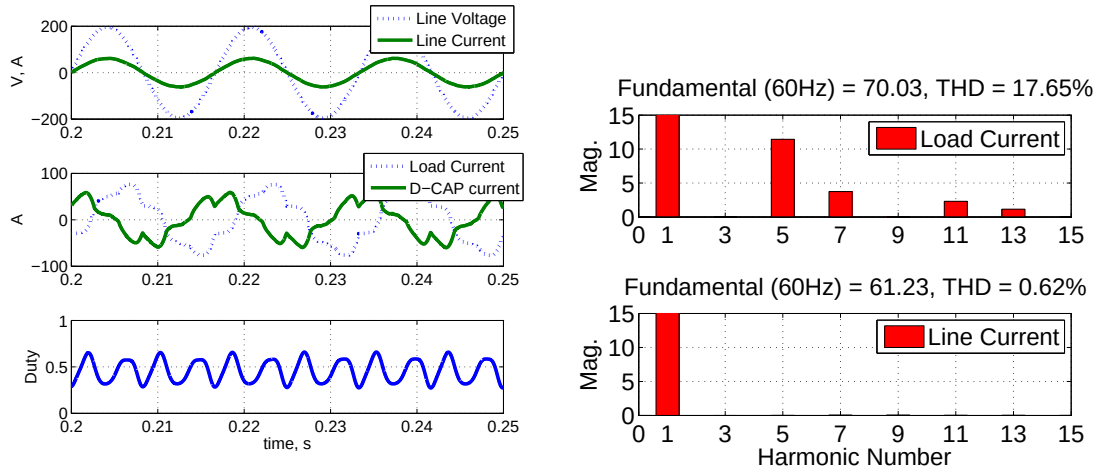
thus preventing the load harmonics from corrupting the voltage at the PCC.

The duty of the switches used to generate the D-CAP current is given by the bottom plot in Figure 7.9(a). The waveform has a very novel characteristic in that it contains only the constant and the even harmonic terms.

Figure 7.10 demonstrates that even under significant distortion of the line voltage, perhaps due to neighboring non-linear loads, the D-CAP is able to decouple the grid dynamics from the load and ensure that only clean sinusoidal current is drawn from the grid. Figure 7.10(b) shows that even though the line voltage has 5.1 percent THD due to the 7th harmonic component, the line current is free of all low-order harmonics.

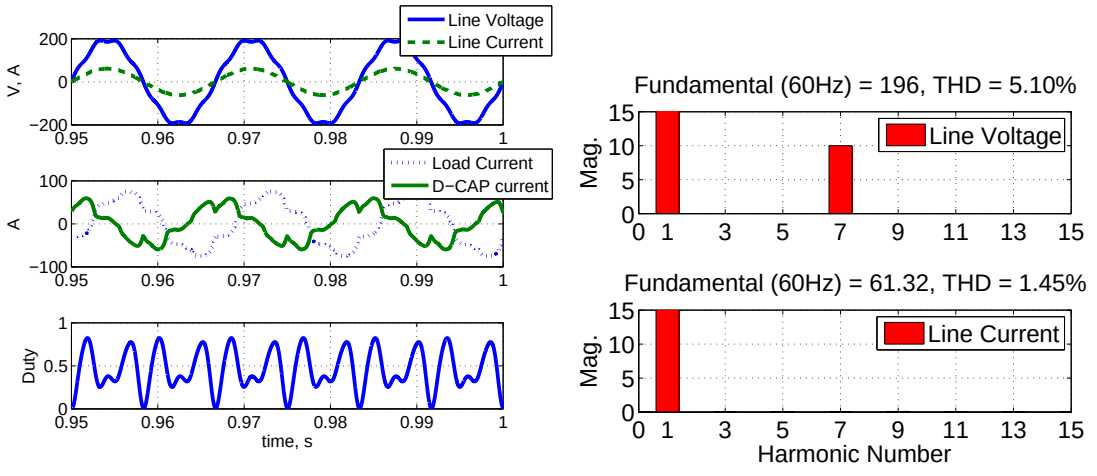
Table 7.3: The selected integral gains for the simulation of the three-phase control architecture applied to the buck D-CAP.

Gain Parameter	Value	Description
G_{1q}	0.5	Q gain of fundamental loop
$[G_{5d}, G_{5q}]$	[1,1]	D/Q gains of the 5th harmonic loop
$[G_{7d}, G_{7q}]$	[0.4,0.4]	D/Q gains of the 7th harmonic loop
$[G_{11d}, G_{11q}]$	[0.5,0.5]	D/Q gains of the 11th harmonic loop
$[G_{13d}, G_{13q}]$	[0.1,0.1]	D/Q gains of the 13th harmonic loop



(a) Time (b) Frequency

Figure 7.9: Simulation results for the three-phase control architecture of the buck D-CAP under nominal line conditions.

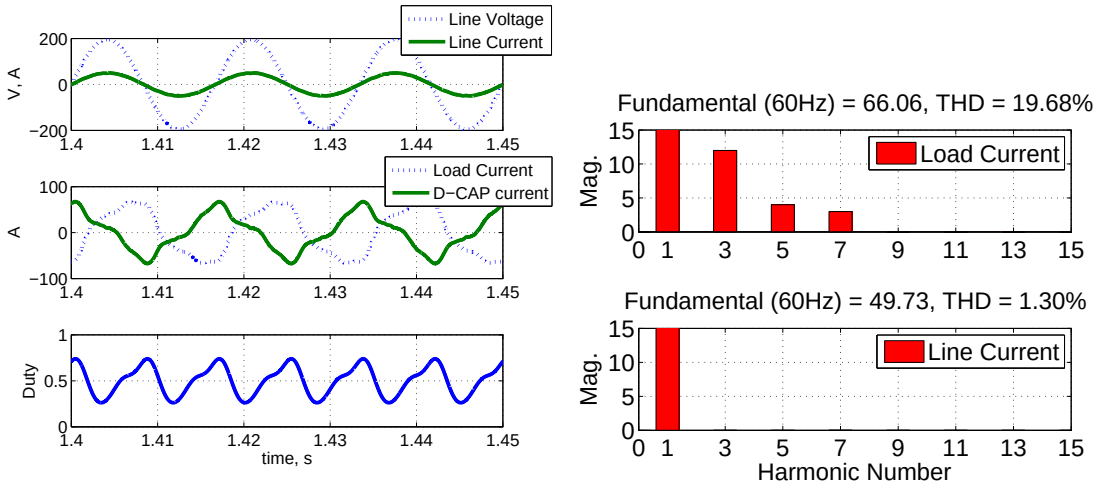


(a) Time (b) Frequency

Figure 7.10: Simulation results for the three-phase control architecture of the buck D-CAP under distorted line conditions.

7.6 Simulation of the Single-Phase Control Architecture

For single-phase systems, or applications where a balanced and symmetrical system cannot be assumed, the single-phase control architecture provides phase-independent control of the three phases. For the operating conditions and component values given in Table 7.2, the simulation results are given by Figure 7.11. The figures indicate that the single-phase controllers are just as effective in mitigating harmonics and improving power factor as their three-phase counterparts.



(a) Time (b) Frequency

Figure 7.11: Simulation results for the single-phase control architecture of the buck D-CAP under nominal line conditions.

7.7 Assessing Stability Through an Example Case Scenario

The stability of the system with the proposed linear controller can be evaluated with the LTI models derived in Chapter 5. However, as the LTI model is derived under operation with a constant duty function, $d(t) = K_0$, the system stability is only determined for the control loop at the fundamental frequency. Alternate approach is required in assessing stability for the harmonic control loops.

For the D-CAP, the primary variable that is being controlled is the Q component of the injected current, I_{Sq}, as it is the Q component that is being driven to zero

with the controller. The previously derived transfer function relating $\tilde{i}_{Sq}$ to the duty function, $\tilde{k}_0$, for the buck D-CAP is,

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{k}_0(s)} = \frac{(P_4^q s^4 + P_3^q s^3 + P_2^q s^2 + P_1^q s + P_0^q)}{\Gamma}, \tag{7.11}$$

where

$$\begin{aligned}
P_4^q &= L^2C^2I_{Lq},\\
P_3^q &= 2RLC^2I_{Lq} + K_0LC^2V_{Sq},\\
P_2^q &= 2\omega^2L^2C^2I_{Lq} - K_0\omega LC^2V_{Sd} + R^2C^2I_{Lq} + K_0RC^2V_{Sq} + 2LCI_{Lq},\\
P_1^q &= K_0CV_{Sq} + 2RCI_{Lq} + K_0\omega^2LC^2V_{Sq} + 2\omega^2RLC^2I_{Lq},\\
P_0^q &= -2\omega^2LCI_{Lq} + K_0\omega CV_{Sd} + \omega^4L^2C^2I_{Lq} + \omega^2R^2C^2I_{Lq}\\
&\quad - K_0\omega^3LC^2V_{Sd} + K_0\omega^2RC^2V_{Sq} + I_{Lq},\\
\Gamma &= L^2C^2s^4 + 2RLC^2s^3 + \left(2\omega^2L^2C^2 + R^2C^2 + 2LC\right)s^2\\
&\quad + \left(2\omega^2RLC^2 + 2RC\right)s + \omega^4L^2C^2 + \omega^2R^2C^2 - \omega^2 2LC + 1.
\end{aligned}$$

The transfer function for the boost is,

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{k}_0(s)} = \frac{P_3^q s^3 + P_2^q s^2 + P_1^q s + P_0^q}{\Gamma}, \tag{7.12}$$

where

$$\begin{aligned}
P_3^q &= LC^2V_{Cq},\\
P_2^q &= RC^2V_{Cq} - \omega LC^2V_{Cd} + K_0^PLCI_{Lq},\\
P_1^q &= \omega^2LC^2V_{Cq} + \left(K_0^P\right)^2CV_{Cq} - 2K_0^P\omega LCI_{Ld} + K_0^PRCI_{Lq},\\
P_0^q &= \left(K_0^P\right)^2\omega CV_{Cd} - \omega^3LC^2V_{Cd} + \omega^2RC^2V_{Cq} - K_0^P\omega^2LCI_{Lq}\\
&\quad - K_0^P\omega RCI_{Ld} + \left(K_0^P\right)^3I_{Lq},\\
\Gamma &= L^2C^2s^4 + 2RLC^2s^3 + \left(2\omega^2L^2C^2 + R^2C^2 + 2\left(K_0^P\right)^2LC\right)s^2\\
&\quad + \left(2\omega^2RLC^2 + 2\left(K_0^P\right)^2RC\right)s + \omega^4L^2C^2 + \omega^2R^2C^2\\
&\quad - 2\left(K_0^P\right)^2\omega^2LC + \left(K_0^P\right)^4,
\end{aligned}$$

$$K_0^P = 1 - K_0.$$

And the transfer function for the buck-boost is given by,

$$\frac{\tilde{i}_{Sq}(s)}{\tilde{k}_0(s)} = \frac{(P_4^q s^4 + P_3^q s^3 + P_2^q s^2 + P_1^q s + P_0^q)}{\Gamma}, \tag{7.13}$$

where

$$\begin{aligned}
P_4^q &= L^2C^2I_{Ld},\\
P_3^q &= 2RLC^2I_{Lq} + K_0LC^2(V_{Sq} + V_{Cq}),\\
P_2^q &= 2\omega^2L^2C^2I_{Lq} - K_0\omega LC^2(V_{Sd} + V_{Cd}) + R^2C^2I_{Lq}\\
&\quad + K_0RC^2(V_{Sq} + V_{Cq}) + 2\left(K_0^P\right)^2LCI_{Lq} + K_0K_0^PLCI_{Lq},\\
P_1^q &= K_0\left(K_0^P\right)^2C(V_{Sq} + V_{Cq}) + 2\left(K_0^P\right)^2RCI_{Lq} + K_0\omega^2LC^2(V_{Sq} + V_{Cq})\\
&\quad + 2\omega^2RLC^2I_{Lq} + K_0K_0^PRCI_{Lq} - 2K_0K_0^P\omega LCI_{Ld},\\
P_0^q &= K_0\left(K_0^P\right)^3I_{Lq} + \omega^4L^2C^2I_{Lq} + \omega^2R^2C^2I_{Lq} + K_0\left(K_0^P\right)^2\omega C(V_{Sd} + V_{Cd})\\
&\quad - 2\left(K_0^P\right)^2\omega^2LCI_{Lq} - K_0\omega^3LC^2(V_{Sd} + V_{Cd}) + K_0\omega^2RC^2(V_{Sq} + V_{Cq})\\
&\quad - K_0K_0^P\omega RCI_{Ld} - K_0K_0^P\omega^2LCI_{Lq} + \left(K_0^P\right)^4I_{Lq},\\
\Gamma &= L^2C^2s^4 + 2RLC^2s^3 + \left(2\omega^2L^2C^2 + R^2C^2 + 2\left(K_0^P\right)^2LC\right)s^2\\
&\quad + \left(2\omega^2RLC^2 + 2\left(K_0^P\right)^2RC\right)s + \omega^4L^2C^2 + \omega^2R^2C^2\\
&\quad - 2\left(K_0^P\right)^2\omega^2LC + \left(K_0^P\right)^4.
\end{aligned}$$

The input filters and line impedances are not considered. The operating conditions and component values are selected and summarized in Table 7.4. The transfer functions are multiplied by an integral compensator, $\frac{G_{1q}}{s}$, to obtain the loop gains and are plotted as root locus and bode plots in Figures 7.12, 7.13, and 7.14 for the buck, boost, and buck-boost respectively. In these figures, the gain of the integral compensators, G_{1q}, for the three configurations are selected such that the closed-loop pole is on the imaginary axis, which constitutes the boundary line for stability. If the

gains are increased further, the poles of the closed-loop systems land on the right-half plane (RHP) and the systems become unstable.

Table 7.4: The operating conditions and the component values selected in assessing the stability of the controllers at the fundamental frequency.

Operating Condition / Component	Value	Unit	Description
$[V_{Sd}\ V_{Sq}\ V_{S0}]$	$[240\sqrt{\frac{2}{3}}\ 0\ 0]$	V	Source Voltage
C	750	μF	Main capacitor
L	50	μH	Switching inductor
R	0.1	Ω	Parasitic resistance
ω	$2\pi 60$	rad/s	Line frequency
K_0	0.5	-	Buck duty
	0.2	-	Boost duty
	0.4	-	Buck-boost duty

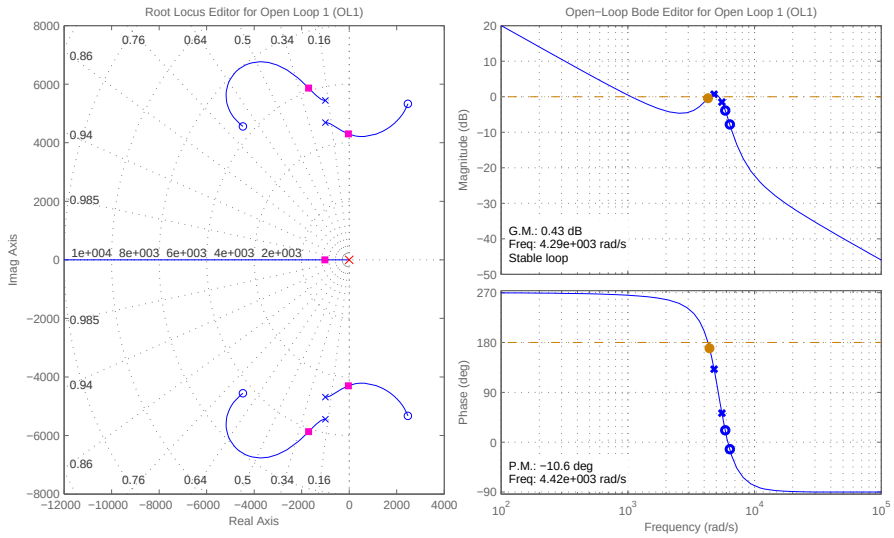


Figure 7.12: Root locus and bode plots of the open-loop transfer function, comprising of the product of the transfer function $\frac{\tilde{i}_{Sq}(s)}{\tilde{k}_0(s)}$ with the compensator $H = \frac{18}{s}$ for the buck D-CAP.

In this example, the upper limits of the gains to keep the buck, boost, and buck-boost systems in the stable region are found to be 18, 4, and 5.5, respectively. As

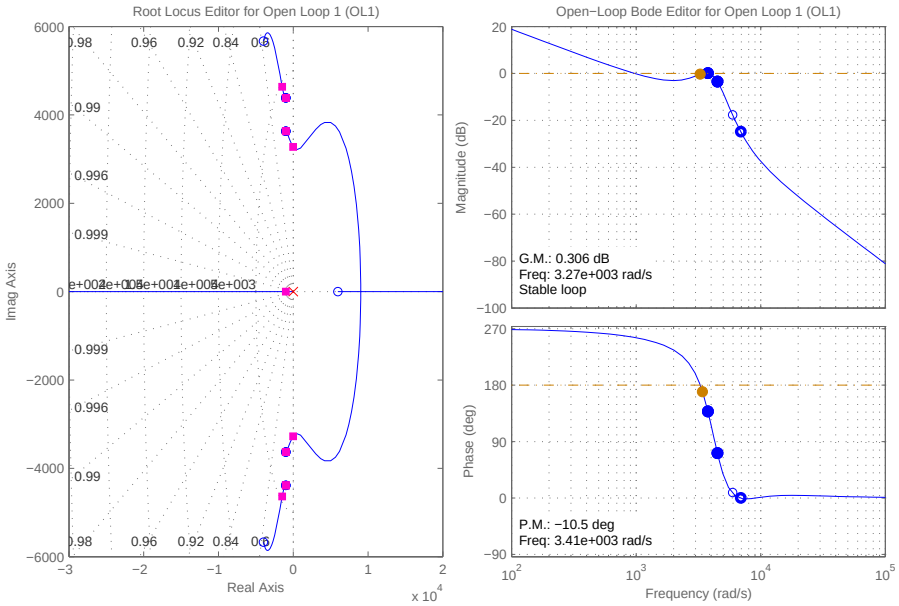


Figure 7.13: Root locus and bode plots of the open-loop transfer function, comprising of the product of the transfer function $\frac{\tilde{i}_{Sq}(s)}{\tilde{k}_0(s)}$ with the compensator $H = \frac{4}{s}$ for the boost D-CAP.

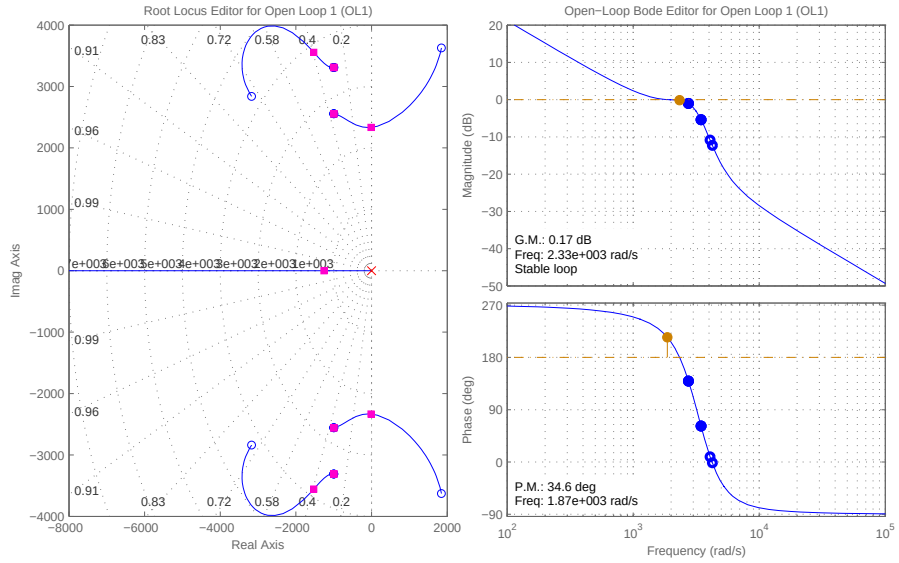


Figure 7.14: Root locus and bode plots of the open-loop transfer function, comprising of the product of the transfer function $\frac{\tilde{i}_{Sq}(s)}{\tilde{k}_0(s)}$ with the compensator $H = \frac{5.5}{s}$ for the buck-boost D-CAP.

long as each of the integral gains is between 0 and the stated upper limits, the closed-loop responses remain stable for the selected operating conditions. To account for tolerances in the operating conditions and component values, the effect of input filter and line impedance, as well as delays and errors in sensors and controllers, adequate gain and phase margins should be provided. Every control design is different, but typically, a minimum phase margin of 45 degrees and gain margin of 5 to 7 dB are necessary. Even larger gain and phase margins may be required to account for all the factors not considered in the transfer functions.

The three example systems are simulated in the time domain using the average models for three different values of integral gain. The three integral gain values are selected as follows:

1. An integral gain that sets the closed-loop poles securely on the left-half plane.

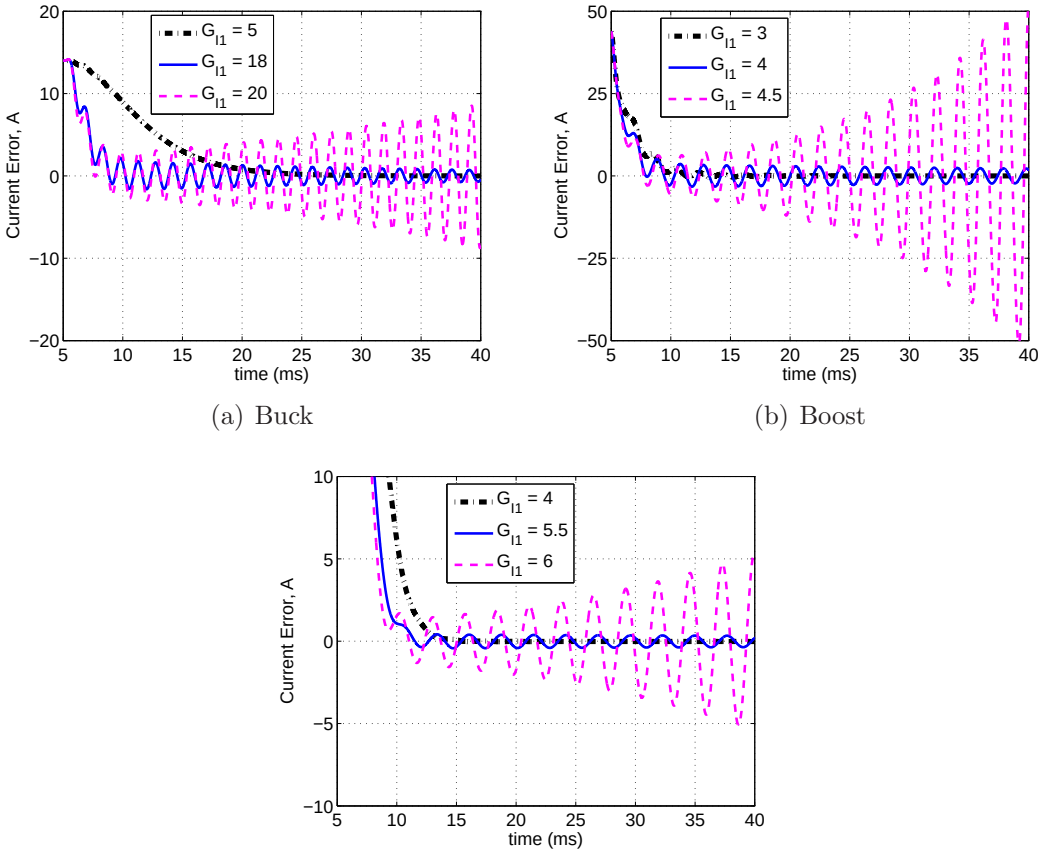
2. An integral gain that sets the closed-loop poles near the imaginary axis.

3. An integral gain that sets the closed-loop poles on the right-half plane.

The Q-component error of the current feeding the integrator is plotted for the three different gain values in Figures 7.15(a),(b), and (c) for the buck, boost, and buck-boost configurations, respectively. For a perfectly tuned controller, the error should be driven to zero as quickly as possible with minimal or no oscillations. As can be assessed from these three sets of time-domain plots, the systems go from stable to unstable right around the gain values predicted by the stability plots of Figures 7.12-7.14.

7.8 Conclusions

The control of the D-CAP is realized through the concept of virtual quadrature sources (VQS) where even harmonic modulation (EHM) terms in combination with a constant term in the duty cycle are used to provide power factor correction and



(a) Buck

(b) Boost

(c) Buck-Boost

Figure 7.15: Time-domain plots of the current error feeding the integrator for gains selected around the stability boundary.

harmonic filtering. However, the control requirements for the D-CAP are quite complex as each EHM term simultaneously affects multiple odd harmonics in the output current, which makes controlling a particular odd harmonic current challenging.

The sensitivity analysis developed in this chapter concluded that the $(n-1)$-th EHM term has the greatest impact upon the n-th odd harmonic current for the buck, the boost, and the buck-boost configurations of the D-CAP. Based on this correlation, single- and three-phase control architectures with linear controllers designed in the synchronous reference frame are presented with an integral compensator at each harmonic of interest. Due to the complex cross-couplings between multiple odd harmonics with any particular even harmonic term in the duty coefficient, full decoupling

is not achievable. Therefore, to minimize the inter-compensator "fighting" in the control system, each control loop is operated with a different time constant. Heuristic guidelines for tuning the time constants of each of the control loops are presented.

The closed-loop operation of the proposed single- and three-phase control architectures are demonstrated using simulations. The results show that the D-CAP systems provide VAR and harmonic compensation with excellent dynamic and steady-state responses.

The stability of the fundamental loops is assessed for the three configurations with their respective transfer functions. Using an example case scenario, the root locus tool in Matlab is employed in graphically finding the point where the D-CAP systems went unstable. By providing adequate phase and gain margins to account for the grid disturbances and impedance of input filter and system that were not accounted for in the transfer functions, a stable closed-loop control can be designed.

CHAPTER VIII

SELECTIVE HARMONIC CULTIVATION

8.1 Introduction

The three most commonly available gate-commutated switching devices for high-power applications not only have limited voltage blocking capability, as highlighted by Figure 8.1, but are also limited in their maximum switching frequency due to thermal constraints and degradation in conversion efficiency at higher frequencies.

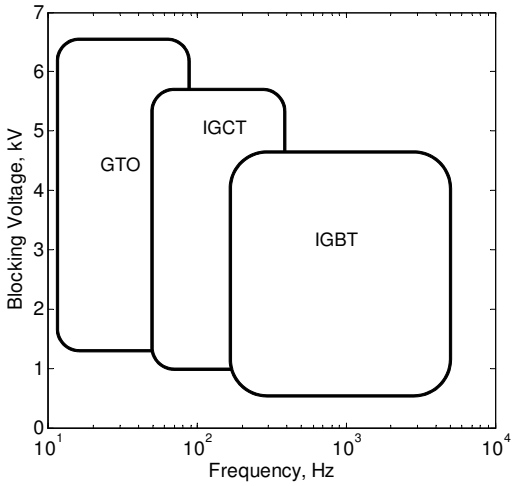


Figure 8.1: Comparison of devices for medium-voltage high-power applications.

The switching frequency of a power semiconductor device is inversely proportional to the size of the device. Thus, while a larger device may be able to block higher voltages and conduct larger current, it invariably operates with a lower switching frequency when compared to a smaller device due to the larger amount of charge that has to be moved around to commutate the device. The rate at which these charges can be moved in and out of the device depends primarily on the thermal management of the system and the device technology. For instance, while a larger IGBT is operated

at 0.5 to 1 kHz to meet certain thermal constraints, a smaller IGBT can be switched as fast as 10 to 20 kHz.

The use of devices with high current ratings but with limited switching frequency, such as IGCTs and large IGBTs, are invariably required for scaling to medium-voltage high-power applications. Operating these devices with carrier-based PWM schemes leads to high THD and poor performance. Specialized modulation schemes based on low switching frequency operation have been proposed previously. The selective harmonic elimination (SHE) and the optimal PWM techniques were established for voltage source inverters to optimize the contribution of each device commutation when operating with a low switching frequency.

The concept of SHE is based on a frequency-domain model of the converter where a complex waveform is represented as a sum of pure sinusoidal waveforms derived using Fourier series. The initial work in SHE for voltage source inverters goes as far back as the mid 1960's [65]. The basic concept is to chop up a square-wave at a fundamental frequency (i.e. 60 Hz) with its infinite harmonic components such that with each additional chop, a particular lower order harmonic is eliminated, until all low-order harmonics, aside from the desired fundamental component, are eliminated up to a certain frequency. At this point, a low-pass filter is employed to filter out the remaining higher order harmonics and pass a relatively clean sinusoidal waveform to the output.

Each commutation is calculated a priori using a frequency-domain model of the converter and is translated to turn-on/turn-off angles for the GTOs/IGCTs. Once the switching harmonics are filtered out, what remains is the desired sinusoidal waveform at the fundamental frequency.

In extending this concept to the DVHCs, the approach has to be modified. Instead of a square-wave at 60 Hz with infinite harmonics that have to be eliminated one at a time, the source voltage for a DVHC is a sinusoidal waveform at 50/60 Hz, from

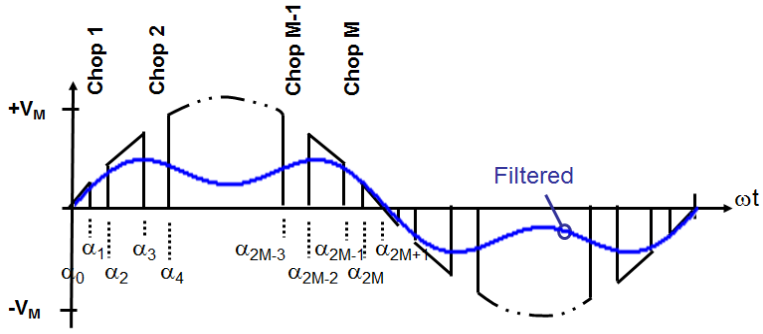
which the desired low-order harmonics have to be 'cultivated' with every chop. The approach is therefore titled 'selective harmonic cultivation' or SHC.

The fundamental operating principles of the DVHCs are also significantly different from that of the VSI. In the DVHC, there are no secondary sources, like the DC source in a VSI. There is only the grid voltage. While the VSI operates by controlling the voltage imposed across the output filter inductor and the subsequent current that is driven across it, the DVHC operates by controlling the equivalent impedance as seen from the grid side. Therefore, the derivation of the optimal firing angles is based on operation with multiple reflections occurring across the switching cell.

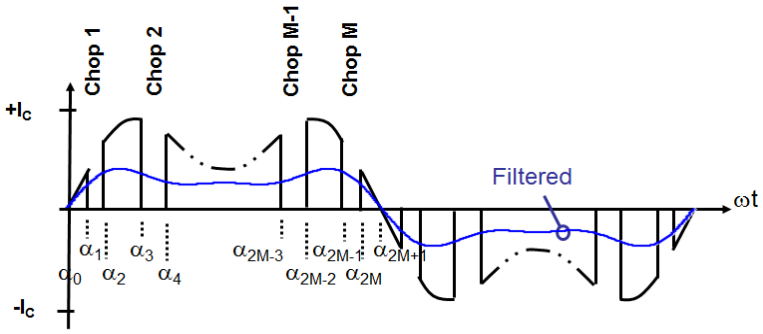
For example, with the buck D-CAP, the source or line voltage is first chopped and impressed across the passive LC components, as depicted in Figure 8.2(a) with the chopping angles, $[\alpha_0, \alpha_1, ..., \alpha_i, ..., \alpha_{2M+1}] \in [0, \pi]$. Subsequently, an average current determined by $i_C(t) = C\mathrm{d}V_C(t)/\mathrm{d}t$ is driven to flow through the capacitor. In turn, this current gets chopped with the exact same firing angles when it is reflected over the switching cell to the line side, as shown in Figure 8.2(b). It is this chopped non-sinusoidal current reflected onto the line side that will provide the desired VAR injection and harmonic filtering.

Unlike an inverter, the same switching function is applied twice to obtain the desired waveform; first to chop the line voltage and then to chop the current induced by the passive network. The non-sinusoidal waveforms in combination with the multiple reflections that occur over filter elements and the switching cell lead to a very large set of non-linear equations that makes solving for the proper firing angles computationally intensive. In the case for boost and buck-boost, the computational resource requirements are even greater.

The optimal PWM concept has been validated to be applicable to the buck D-CAP with detailed mathematical derivation and validation of the theory presented in [71]. This work is simplified for operation in the utility grid environment and



(a) Chopped line voltage across the passive kernel.



(b) Chopped passive kernel's current injected into the grid.

Figure 8.2: Optimal PWM techniques applied to dynamically vary the impedance of the passive component and inject controlled VAR and harmonic currents into the line.

extended to both the boost and the buck-boost configurations in this chapter.

8.2 Modeling of the Switching Cell

The frequency models of the DVHC systems have already been discussed in Section 6. In order to modify that model for the SHC technique, the matrices, T_1, and T_2, are replaced with ones that take into account the low switching frequency operation of the converter where the firing angles, α_i, provide the control handles, instead of the even harmonic coefficients of the duty function.

Any 2π-periodic and integrable function, $f(\omega t)$, can be represented as a partial sum of sine and cosine terms, called the Fourier series of $f(\omega t)$, as follows:

$$f(\omega t) = \frac{a_0}{2} + \sum_{h=1}^{\infty} [a_h \sin(h\omega t) + b_h \cos(h\omega t)], \tag{8.1}$$

where

$$a_h = \frac{1}{\pi}\int_0^{2\pi} f(\omega t)\sin(h\omega t)\,d(\omega t), \tag{8.2}$$

$$b_h = \frac{1}{\pi}\int_0^{2\pi} f(\omega t)\cos(h\omega t)\,d(\omega t). \tag{8.3}$$

Since this work is dealing with a direct AC converter without any DC voltage or current present, the constant term in the Fourier series is not considered.

The switching cell of the DVHC can chop up a voltage or current waveforms with an arbitrary number of harmonics. A frequency model of the switching cell, T, should be able to take the Fourier coefficients of a voltage or current vector,

$$V = \left[\underbrace{V_1 ... V_{N_H}}_{cos}\underbrace{V_1 ... V_{N_H}}_{sin}\right] \tag{8.4}$$

$$I = \left[\underbrace{I_1 ... I_{N_H}}_{cos}\underbrace{I_1 ... I_{N_H}}_{sin}\right] \tag{8.5}$$

and generate a new set of Fourier coefficients that are representative of the chopped-up waveform.

The Fourier coefficients of the chopped-up waveform for the harmonic number h are derived based on:

$$a_h = a_{gh} + c_{gh}, \tag{8.6}$$

$$b_h = b_{gh} + d_{gh}, \tag{8.7}$$

where:

$$a_{gh} = \frac{2}{\pi}\int_0^{\pi} U_{Cg}\cos(g\omega t)\cos(h\omega t)\,d(\omega t), \tag{8.8}$$

$$b_{gh} = \frac{2}{\pi}\int_0^{\pi} U_{Cg}\cos(g\omega t)\sin(h\omega t)\,d(\omega t), \tag{8.9}$$

$$c_{gh} = \frac{2}{\pi}\int_0^{\pi} U_{Sg}\sin(g\omega t)\cos(h\omega t)\,d(\omega t), \tag{8.10}$$

$$d_{gh} = \frac{2}{\pi}\int_0^{\pi} U_{Sg}\sin(g\omega t)\sin(h\omega t)\,d(\omega t), \tag{8.11}$$

$U_{Cg} \equiv$ Cosine coefficient of the g^{th} harmonic of the input waveform,

$U_{Sg} \equiv$ Sine coefficient of the g^{th} harmonic of the input waveform.

Applying trigonometric identities, evaluating the integrals for the chopping angles, $[\alpha_0, \alpha_1, ..., \alpha_i, ..., \alpha_{2M+1}] \in [0, \pi]$, and rearranging the result as a matrix product, $T_1 \cdot U^T$, where U is the one-dimensional matrix with the input waveform's Fourier coefficients, $U = [U_{C1}...U_{CN_H}\ U_{S1}...U_{SN_H}]$, the frequency model, T_1, is derived:

$$T_1 = \left[\begin{array}{cc} A_1 & C_1 \\ B_1 & D_1 \end{array} \right]_{2N_H \times 2N_H}, \tag{8.12}$$

where the sub-matrix A_1 is given by,

$$A_1(n,m) = \begin{cases} \frac{1}{\pi} \sum_{i=1}^{N_S} (-1)^i \left[\frac{\sin(2g\alpha_i)}{2g} + \alpha_i \right] & \text{for } g = h, \\ \frac{1}{\pi} \sum_{i=1}^{N_S} (-1)^i \left[\frac{\sin((g+h)\alpha_i)}{g+h} + \frac{\sin((g-h)\alpha_i)}{g-h} \right] & \text{for } g \neq h, \end{cases} \tag{8.13}$$

the sub-matrix B_1 is given by,

$$B_1(n,m) = \begin{cases} \frac{1}{\pi} \sum_{i=1}^{N_S} (-1)^i \left[\frac{-\cos(2g\alpha_i)}{2g} \right] & \text{for } g = h, \\ \frac{1}{\pi} \sum_{i=1}^{N_S} (-1)^i \left[\frac{-\cos((g+h)\alpha_i)}{g+h} + \frac{\cos((g-h)\alpha_i)}{g-h} \right] & \text{for } g \neq h, \end{cases} \tag{8.14}$$

the sub-matrix C_1 is given by,

$$C_1(n,m) = \begin{cases} \frac{1}{\pi} \sum_{i=1}^{N_S} (-1)^i \left[\frac{-\cos(2g\alpha_i)}{2g} \right] & \text{for } g = h, \\ \frac{1}{\pi} \sum_{i=1}^{N_S} (-1)^i \left[\frac{-\cos((g+h)\alpha_i)}{g+h} - \frac{\cos((g-h)\alpha_i)}{g-h} \right] & \text{for } g \neq h, \end{cases} \tag{8.15}$$

and the sub-matrix D_1 is given by,

$$D_1(n,m) = \begin{cases} \frac{1}{\pi} \sum_{i=1}^{N_S} (-1)^i \left[\frac{-\sin(2g\alpha_i)}{2g} + \alpha_i \right] & \text{for } g = h, \\ \frac{1}{\pi} \sum_{i=1}^{N_S} (-1)^i \left[\frac{-\sin((g+h)\alpha_i)}{g+h} + \frac{\sin((g-h)\alpha_i)}{g-h} \right] & \text{for } g \neq h, \end{cases} \tag{8.16}$$

for

$$g = 2m - 1,$$

$$h = 2n - 1,$$

$$m = \{1, ..., N_H\},$$

$$n = \{1, ..., N_H\},$$

$$\alpha_i \equiv i^{th} \text{ firing angle},$$

$$N_H \equiv \text{total number of harmonics considered},$$

$$N_S \equiv \text{total number of firing angles considered}.$$

The matrix, T_1, is able to model the switching behavior in the boost DVHCs as well, but the matrix is re-labeled as T_2 because the solution-set is equivalent to the complementary duty cycle, $(1 - d(t))$. For the buck-boost DVHCs, T_2, is derived in similar fashion but the chopped waveform generated by T_2 is complementary: what was low is high, and what was high is low. The model is given by,

$$T_2 = \begin{bmatrix} A_2 & C_2 \\ B_2 & D_2 \end{bmatrix}_{2N_H \times 2N_H}, \tag{8.17}$$

where the sub-matrix A_2 is given by,

$$A_2(n,m) = \begin{cases} \frac{1}{\pi} \sum_{i=2}^{N_S-1} (-1)^{(i-1)} \left[\frac{\sin(2g\alpha_i)}{2g} + \alpha_i \right] & \text{for } g = h, \\ \frac{1}{\pi} \sum_{i=2}^{N_S-1} (-1)^{(i-1)} \left[\frac{\sin((g+h)\alpha_i)}{g+h} + \frac{\sin((g-h)\alpha_i)}{g-h} \right] & \text{for } g \neq h, \end{cases} \tag{8.18}$$

the sub-matrix, B_2, is given by,

$$B_2(n,m) = \begin{cases} \frac{1}{\pi} \sum_{i=2}^{N_S-1} (-1)^{(i-1)} \left[\frac{-\cos(2g\alpha_i)}{2g} \right] & \text{for } g = h, \\ \frac{1}{\pi} \sum_{i=2}^{N_S-1} (-1)^{(i-1)} \left[\frac{-\cos((g+h)\alpha_i)}{g+h} + \frac{\cos((g-h)\alpha_i)}{g-h} \right] & \text{for } g \neq h, \end{cases} \tag{8.19}$$

the sub-matrix, C_2, is given by,

$$C_2(n,m) = \begin{cases} \frac{1}{\pi} \sum_{i=2}^{N_S-1} (-1)^{(i-1)} \left[\frac{-\cos(2g\alpha_i)}{2g} \right] & \text{for } g = h, \\ \frac{1}{\pi} \sum_{i=2}^{N_S-1} (-1)^{(i-1)} \left[\frac{-\cos((g+h)\alpha_i)}{g+h} - \frac{\cos((g-h)\alpha_i)}{g-h} \right] & \text{for } g \neq h, \end{cases} \tag{8.20}$$

and the sub-matrix, D_2, is given by by,

$$D_2(n,m) = \begin{cases} \frac{1}{\pi}\sum_{i=2}^{N_S-1}(-1)^{(i-1)}\left[\frac{-\sin(2g\alpha_i)}{2g} + \alpha_i\right] & \text{for } g = h, \\ \frac{1}{\pi}\sum_{i=2}^{N_S-1}(-1)^{(i-1)}\left[\frac{-\sin((g+h)\alpha_i)}{g+h} + \frac{\sin((g-h)\alpha_i)}{g-h}\right] & \text{for } g \neq h, \end{cases} \tag{8.21}$$

8.3 Formulation of the Non-Linear Equations

Accounting for the input filter, the following non-linear matrix equations are solved to obtain the desired reference current, I_S^*, with respect to the firing angles, α_i, for the three configurations of the D-CAP:

$$G = \begin{cases} \left[F_{21} + F_{22}T_1Y_{RLC}T_1\Psi_1^{-1}F_{11}\right]V_S^T - I_S^{*T} = 0 & \text{buck}, \\ \left[F_{21} + F_{22}\Theta^{-1}Y_{RL}\Psi_2^{-1}F_{11}\right]V_S^T - I_S^{*T} = 0 & \text{boost}, \\ \left[F_{21} + F_{22}T_1\Theta^{-1}Y_{RL}T_1\Psi_3^{-1}F_{11}\right]V_S^T - I_S^{*T} = 0 & \text{buck-boost}, \end{cases} \tag{8.22}$$

where

$$\Theta = \left(\mathrm{I} + Y_{RL}T_2Z_CT_2\right),$$

$$\Psi_1 = \left(\mathrm{I} - F_{12}T_1Y_{RLC}T_1\right),$$

$$\Psi_2 = \left(\mathrm{I} - F_{12}\Theta^{-1}Y_{RL}\right),$$

$$\Psi_3 = \left(\mathrm{I} - F_{12}T_1\Theta^{-1}Y_{RL}T_1\right),$$

$F_{xy} \equiv$ Two-port model of the input filter,

$Y_{RLC} \equiv$ Admittance model of the series-connected RLC components,

$Z_C \equiv$ Impedance model of the capacitor, C,

$Y_{RL} \equiv$ Admittance model of the RL components used in boost and buck-boost configuration,

$I_S^* \equiv$ Desired source or injected current.

The impedance and admittance matrices derived in Chapter 6 can be used directly here.

The Jacobian of the non-linear function, G, is derived based on:

$$J = \left[\frac{dG}{d\alpha_0} \; \frac{dG}{d\alpha_1} \; \cdots \; \frac{dG}{d\alpha_i} \; \cdots \; \frac{dG}{d\alpha_{N_S}} \right]. \tag{8.23}$$

In selecting the coefficients of the desired current, the underlying concept of VQS is considered. The harmonics to be controlled are constrained by the desired or reference values, while the other harmonics must be left unconstrained such that energy can be exchanged between these "don't care" harmonics and the desired ones.

For example, to compensate for the harmonics generated by a three-phase diode-rectifier load, the following non-linear equations are solved for the angle vector $\mathbf{x} = [\alpha_0, \alpha_1, ..., \alpha_i, ..., \alpha_{N_S-1}] \in [0, \pi]$:

$$\begin{aligned}
0 &= I_{S1|\cos}(\mathbf{x}) - I^*_{S1|\cos}, \\
0 &= I_{S5|\cos}(\mathbf{x}) - I^*_{S5|\cos}, & 0 &= I_{S5|\sin}(\mathbf{x}) - I^*_{S5|\sin}, \\
0 &= I_{S7|\cos}(\mathbf{x}) - I^*_{S7|\cos}, & 0 &= I_{S7|\sin}(\mathbf{x}) - I^*_{S7|\sin}, \\
0 &= I_{S11|\cos}(\mathbf{x}) - I^*_{S11|\cos}, & 0 &= I_{S11|\sin}(\mathbf{x}) - I^*_{S11|\sin}, \\
0 &= I_{S13|\cos}(\mathbf{x}) - I^*_{S13|\cos}, & 0 &= I_{S13|\sin}(\mathbf{x}) - I^*_{S13|\sin}, \\
0 &= I_{S17|\cos}(\mathbf{x}) - I^*_{S17|\cos}, & 0 &= I_{S17|\sin}(\mathbf{x}) - I^*_{S17|\sin},
\end{aligned}$$

where the starred components, $I^*_{Sh|\cos}$ and $I^*_{Sh|\sin}$, are equal in magnitude but in anti-phase with the harmonics generated by the load. Triplen harmonics, or harmonics that are a multiple of three, do not exist in a three-wire three-phase system, and as such, these harmonic components are left unconstrained. Further, all harmonics above the 17th are also considered to be unconstrained in this example.

When operating the DVHCs with the commutation angles specified by the solution, $\mathbf{x}$, a current with the specified harmonic components are synthesized to cancel out the load harmonics. However, the DVHCs also synthesize components at the unconstrained harmonics. In the case of the triplen harmonics, they naturally cancel in

a three-wire three-phase system. For the harmonics above the 17th in this example, a low-pass input filter can suppress their injection into the grid.

In single-phase systems or four-wire three-phase systems, triplen harmonics do not cancel and therefore need to be constrained appropriately. If a load or a system is consuming reactive power at these harmonics, then the references when solving the non-linear equations are set to equal the amount of compensation required. Otherwise, these harmonics are constrained to be zero such that they are not synthesized by the DVHCs. In these systems, the unconstrained harmonics are typically chosen to be above the highest harmonic requiring compensation and are suppressed with a low-pass input filter.

The number of commutation angles, N_S, within half a line cycle to compensate for up to N_H number of harmonics is selected based on:

$$N_S \geq \begin{cases} 2\,(N_H+2) & \text{for the buck,} \\ 4\,(N_H+2) & \text{for the boost,} \\ 8\,(N_H+2) & \text{for the buck-boost.} \end{cases} \tag{8.24}$$

The non-linear equations can be solved using the Newton/Rapshon technique outlined in Section 6.8, or using the built-in root-finding 'fsolve' function in Matlab.

8.4 Example Case Scenario

The SHC technique is demonstrated using a buck-boost D-CAP operating in a single-phase system. The operating conditions and component values of the D-CAP are given by Table 8.1. The source impedance, L_S, is omitted in this example for simplicity as the equivalent input filter would have been a fourth-order filter with the source impedance taken into account. Harmonics up to 11th are compensated in this example, resulting in 64 firing angles every half line cycle or an equivalent switching frequency of about 3.8 kHz. The Matlab script used to calculate the firing angles are given in Appendix A. The direct term at the fundamental frequency is unconstrained.

The results are presented in Table 8.2, where the harmonics in the injected current are compared against the reference harmonics. The current through the switching inductor, L_{F2}, and voltage across the main capacitor, C, are depicted by Figure 8.3.

Table 8.1: The selected operating conditions and the component values for a buck-boost D-CAP for validating the effectiveness of selective harmonic cultivation.

Operating Condition / Component	Value	Unit	Description
V_S	$480\sqrt{\frac{2}{3}}$	V	Source voltage
C	2.3	mF	Main capacitor
C_{F1}	50	μF	Input filter capacitor 1
C_{F2}	1.3	mF	Input filter capacitor 2
L_{F1}	2.2	μH	Input filter inductor
R_{L1}	0.1	Ω	Parasitic resistance
L_{F2}	191	μH	Switching inductor
R_{L2}	0.1	Ω	Parasitic resistance

Table 8.2: Comparison of the reference and the synthesized current harmonics for a buck-boost D-CAP when operating with selective harmonic cultivation.

Harmonic Term	Reference	FFT of Simulation	$\|$Error$\|$
$I_{S1\|\cos}$	450	446	0.89%
$I_{S3\|\cos}$	100	99.6	0.4%
$I_{S3\|\sin}$	0	0.0	N/A
$I_{S5\|\cos}$	0	-0.350	N/A
$I_{S5\|\sin}$	100	100	0%
$I_{S7\|\cos}$	100	98.4	1.6%
$I_{S7\|\sin}$	0	-0.859	N/A
$I_{S9\|\cos}$	0	-1.91	N/A
$I_{S9\|\sin}$	50	49.7	0.6%
$I_{S11\|\cos}$	0	-1.49	N/A
$I_{S11\|\sin}$	0	-0.319	N/A

8.5 Limitations of SHC

Figure 8.4(a) demonstrates results of the SHC for a buck D-CAP topology with maximum fundamental VAR rating of 120 kVA per phase with a line-to-neutral voltage

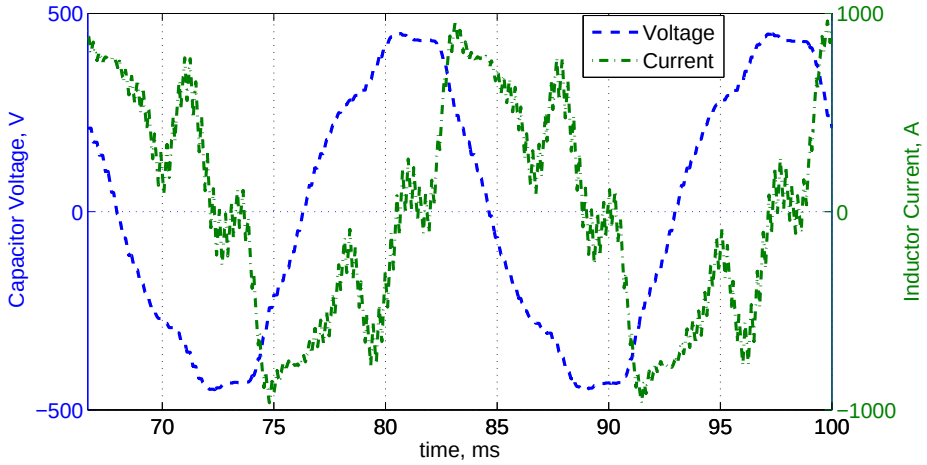
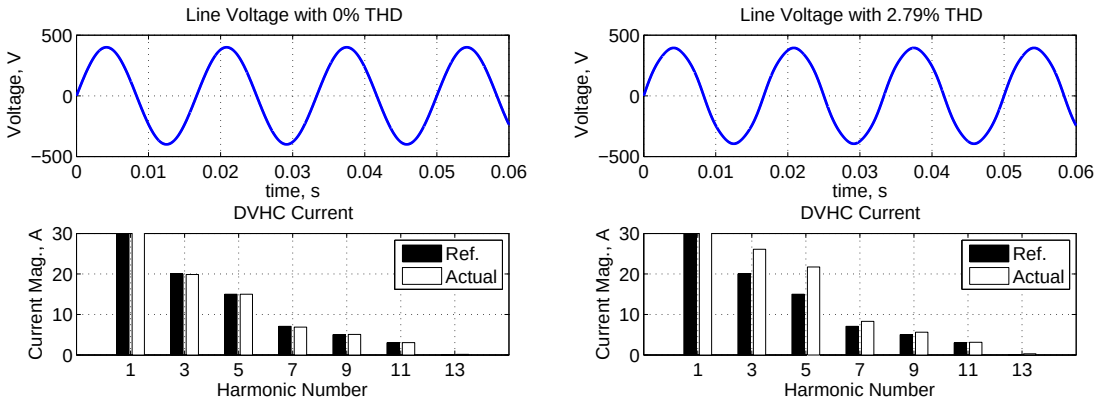


Figure 8.3: Voltage across the main capacitor and current through the switching inductor of a buck-boost D-CAP when it is operated with SHC and compensating up to the 11th harmonic.

of 400 V. As long as the line voltage and the amount of VAR and harmonic compensation requirements are fixed, and the system impedances are well known and remain constant, SHC based on off-line calculations is able to accurately deliver the right amount of fundamental and harmonic currents, as depicted in the figure.



(a) Line voltage with 0% THD

(b) Line voltage with 2.79% THD

Figure 8.4: Simulation results showing the grid voltage and FFT of the current injected by the DVHC converter when operated with SHC.

Unfortunately, system impedances do not remain fixed, and the reactive power

requirements of the load vary throughout the day. Figure 8.4(b) demonstrates the operation of the same converter with the same firing angles but with a slight degree of harmonics now present in the line voltage. As is observable in the figure, for the same firing angles that were tuned offline, the injected harmonics no longer match the desired reference. Thus, it is critical that the firing angles be tunable while the converter is in operation to compensate for the dynamic nature of the grid and the load.

Another limitation lies in the design of the input filter and the switching inductor, whose size are dictated by the effective switching frequency of the converter. The lower the effective switching frequency, the larger these passive components. This limitation has been addressed in inverter-based STATCOMs through multi-pulse designs employing phase-shifted transformers [80], which reduce the size of the required passive components at the cost of low-frequency transformers.

The effective switching frequency also limits the maximum harmonics that can be compensated. Typically, the number of firing angles is selected based on the highest harmonics to be compensated, which include the terms that need to be constrained to zero. For example, if the highest harmonic is the fifth, the effective switching frequency is selected at around 3 kHz. This implies that all the odd harmonics between 0.3 to 3 kHz should be constrained to zero to minimize the rating and size of the input filter. Conversely, if a device with maximum switching frequency of 1 kHz is selected, then the maximum firing angles is limited to about 16 every half line cycle. This in turns limits the maximum harmonics to within 100 Hz, which implies that only the fundamental reactive power can be supplied at this switching frequency.

8.6 Conclusions

An approach to controlling the DVHCs, and in particular, the D-CAP when operated with low switching frequency is presented in this chapter. Semiconductor switches like

IGCTs, GTOs/ETOs, and large IGBTs cannot operate with high switching frequency due to their thermal constraints. Attempting to operate these devices with pulse-width modulation (PWM) and duty-cycle control techniques under low switching frequency can lead to generation of waveforms with poor THD.

When there is a limited number of switch commutations available to synthesize a waveform with a particular set of harmonics, every commutation has to be as optimal as possible. Selective harmonic cultivation technique is presented in this chapter that calculates the optimal angle at which the commutations should occur to generate the current with the desired harmonics.

The effective switching frequency should be selected to be 10 to 20 times the highest harmonic being compensated. So, for purely fundamental VAR injection at 60 Hz, the switching frequency is set to 600 Hz. With third harmonic filtering, the switching frequency is set to 1800 Hz. Conversely, with the large devices limited to a certain switching frequency, f_S, the highest harmonic that can be compensated has to be less than $f_S/10$. The decade factor ensures that the energy at the switching frequency do not interact with the compensated harmonics. It also reduces the requirements on the filters, making them smaller and more effective in suppressing the switching harmonics.

The primary limitation of the SHC technique is that it is very computationally intensive and thus may not be suitable in dynamic applications where the load and diversity profile of the system are constantly in flux. To enable real-time control of the DVHCs, significant computing resources need to be installed on-site that senses the various voltages and currents, calculates the harmonic coefficients, solves the non-linear equations, and outputs the optimal commutation angles. While there have been techniques such as equal area criteria for VSIs that attempt to provide real-time calculation of the optimal angles with significantly reduced computational requirements [85, 82, 49], due to the complex operation, similar techniques have not

yet been developed for the DVHCs.

Until a real-time technique is developed, look-up tables with pre-calculated commutation angles may be utilized for different operating conditions. This is an approach that has been employed in VSIs when operated with selective harmonic elimination. However, while this approach will be quite effective for fundamental VAR compensation where the phase angle of the fundamental current remains fixed with only the magnitude changing, it may not work as well for harmonic filtering, where both the phase angles and magnitude can change within a short period of time, requiring a significantly larger table of commutation angles.

Aside from this limitation, which will soon be obsolete due to more robust and powerful floating-point processors coming into the market at lower costs, the SHC technique presented in this chapter demonstrated that with a good model of the converter and the surrounding system, the DVHCs can inject current with precisely controlled harmonics when devices are operated with a low switching frequency.

CHAPTER IX

SCALING TO MEDIUM VOLTAGES

9.1 Introduction

To scale the design of the direct AC converters to realistic grid voltage levels, and to do so without low frequency transformers, requires operation at voltages from 2 kV to over 35 kV. Even with the eventual availability of high-voltage (>10 kV) silicon-carbide (Si-C) devices, a large number of series-connected devices would still be required. Today's industrial voltage source inverters (VSIs) use multi-level and cascaded single-phase configurations to operate at medium voltages. These topologies not only facilitate scaling to higher voltage levels, but by allowing multiple voltage levels to be synthesized, output with lower harmonic contents and units with smaller passive filters are achievable.

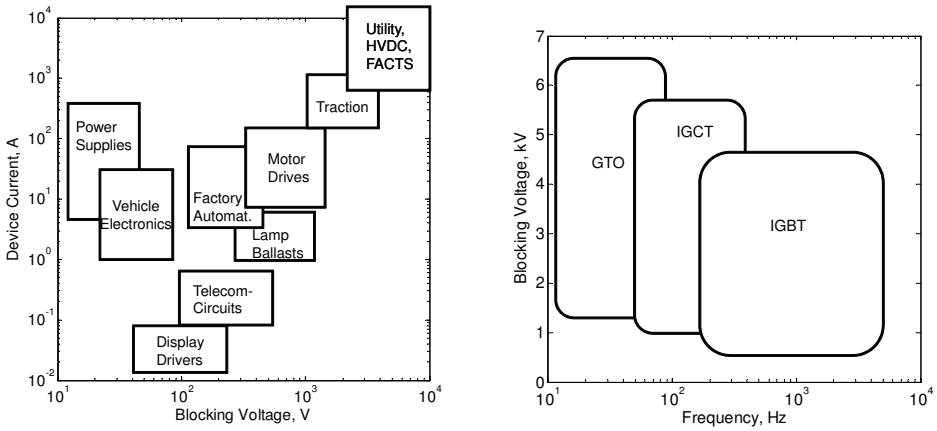
Significant research has been done on the concept of modular power electronic building blocks (PEBBs) for the VSIs. These are typically configured with two power devices in the format of an inverter pole, with control, sensing, and protection all packaged together. The PEBBs are designed to be interconnected to allow scaling through series connection for voltage, and parallel connection for current. Similar strategy in realizing an AC PEBB topology can lead to a modular, robust, and a cost-effective approach to scaling direct AC converters, like the D-CAP, to higher voltages.

This chapter presents several modular approaches to scale the D-CAP to higher voltages with simulation results validating their good performance. The fundamental principles underlying the methodologies used in scaling are similar to commercial approaches to scaling the VSIs. However, due to the nature of direct AC converters,

which employ AC switches, as well as the differences in the operating characteristics between DVHCs and VSIs, implementations of the hardware and controls are very different.

9.2 Limitations of Semiconductor Switches

Semiconductor switch ratings for various applications are given by Figure 9.1(a) where line voltages of over 10 kV are common for most utility-grid applications. However, the three most commonly available silicon-based devices for high power applications have limited voltage blocking capability as highlighted by Figure 9.1(b).



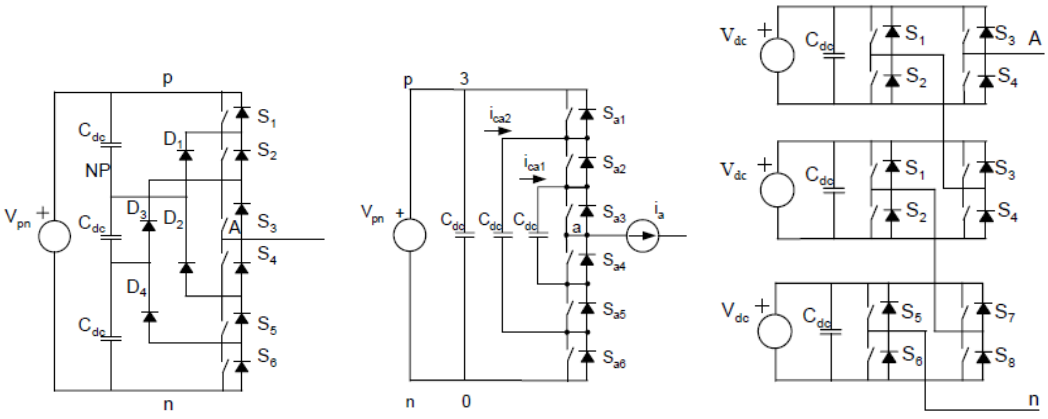
(a) Power applications (b) Power switches

Figure 9.1: Application requirements versus available devices.

Series connecting fractionally-rated devices to realize an equivalent switch of a higher voltage rating is one approach to address the limited blocking voltage capability of the existing devices. However, robust and efficient means to ensure static and dynamic voltage sharing have often led to very complex gate driver designs.

Multi-level topologies in Figure 9.2 were introduced as simple and reliable alternatives for scaling the VSIs to medium voltages. The three topologies are known as a neutral-clamped (or diode-clamped), a flying capacitor, and a cascaded full-bridge, and are found in many commercial products from active filters to STATCOMs

[70, 53, 89, 55, 84, 52, 16, 47]. These three inverter topologies, if represented with ideal switches, share the same configuration as the D-CAP. Therefore, a dual of each of these configurations should also exist where the input voltage is provided by an AC instead of a DC source.



(a) Diode-Clamped (b) Flying Capacitor (c) Cascaded Cells

Figure 9.2: The three popular approaches to implementing multi-level VSIs with a DC input.

The operation of the neutral-clamped topology is predicated upon a multi-phase implementation to charge balance the capacitors. This poses a serious limitation as the DVHCs are implemented on a single-phase basis for sourcing asymmetrical and unbalanced VAR and harmonic compensation. Therefore, the other two topologies are considered as they are more amenable to reconfigurations.

9.3 Challenges in Scaling with Direct AC Converters

The design of the VSIs, which is at the heart of most grid-connected FACTS and HVDC Light converters, allows for a turn-off of individual or all devices when fault current levels are detected. The presence of reverse conducting diodes allows a path for the current to flow, even as the main semiconductor devices are turning off. This safe mode of turn-off in the presence of unanticipated faults is at the heart of the technology's robustness. In the case of direct AC converters, such as the matrix

converter, turning off a single device in the presence of high fault currents can lead to catastrophic device destruction unless polarized snubbers are provided around each device.

Safe switching in an AC-AC converter mandates a complex multi-step switching pattern that is based on voltage and/or current polarity [87, 88]. This is especially challenging around the zero-crossing points, where the sensors may be unable to accurately assess the polarity, especially with a high level of harmonics. An error in the current or voltage measurements can result in sequencing of the wrong switching pattern, which can either momentarily interrupt the current path in a current-based commutation, leading to a large voltage spike, or short-circuit the capacitors and/or voltage sources in a voltage-based commutation, drawing a large amount of current well above the thermal ratings of the devices and components. Both conditions can permanently damage the devices and disable the converter entirely. Figure 9.3 demonstrates the synthesized voltage across the passive component when the DVHC is operated without a snubber under current-based commutation. A large spike is seen around the zero-crossings of the current due to inadequate accuracy of the sensor. Errors in measurements invariably exist but the design of the converter needs to be robust enough such that these errors do not degrade the performance or the life of the converter.

A popular snubber configuration used with matrix converters is depicted in Figure 9.4(a) where two diode bridges feed a DC regulated snubber capacitor [59]. Although this circuit provides effective snubbing of the filter and parasitic currents, every time energy is snubbed, the circuit induces a spike in the synthesized waveform with magnitude equal to the snubber capacitor voltage. The same diode snubber concept applied to a single-phase AC chopper circuit is depicted in Figure 9.4(b). The operation of the snubber is demonstrated in Figure 9.4(c). The figure shows large but clamped spikes around the zero-crossing regions of the current. These spikes, even in the presence of

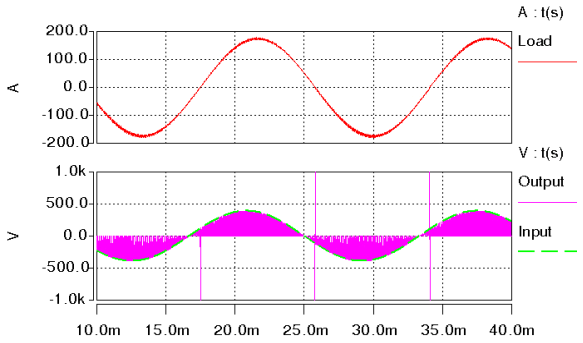


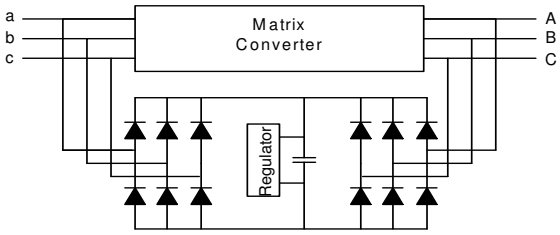
Figure 9.3: Operation of a two-level DVHC with (top) current through filter inductor, and (bottom) chopped up input voltage across the output exhibiting voltage impulses due to improper device commutations that disrupt the current path.

a snubber circuit, are undesirable. The snubber circuit is also inherently unsuitable for scaling to higher voltage levels without a multi-level topology of its own.

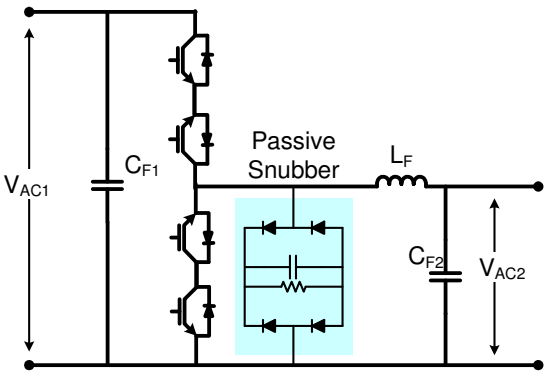
The high diode count of the snubber used in the matrix converters led to the development of an alternate configuration with half the number of diodes, but with essentially the same characteristics and effectiveness. The primary devices' anti-parallel diodes are leveraged to provide low-impedance channels for the snubbed energy [61]. This was achieved through the pairing of common-emitter and common-collector arrangements of the bi-directional switches to direct the energy to the snubber capacitor as shown in Figure 9.5.

While the snubbers of Figures 9.4 and 9.5 are able to ensure devices are protected against incorrect switching sequence and fault events that require the devices to be suddenly turned off, these snubber circuits have a few major limitations that make it difficult to use them when scaling to higher voltages. These limitations are summarized as follows:

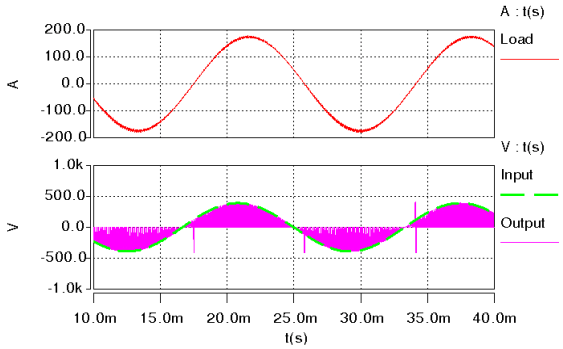
1. Every time the snubber operates, a spike equal to the magnitude of the snubber DC voltage is reflected across the input and/or output. If the spikes occur frequently enough from incorrect commutation sequences, they can degrade the performance of the converter.



(a) Diode-bridge snubber used with matrix converter



(b) Diode snubber used in matrix converter applied to an AC chopper cell



(c) Operation of a two-level DVHC with (top) current through filter inductor, and (bottom) chopped up input voltage exhibiting clamped voltage spikes due to activation of the diode snubber.

Figure 9.4: The use of a passively-regulated diode snubber provides safe commutations in a direct AC-AC converter but still exhibits spikes.

2. As the converter itself is scaled up in voltage and power, the snubber circuit must be able to scale up as well with fractionally-rated devices and passive components, and with reasonable basic insulation levels (BIL). It is not clear how this can be achieved with these two snubber designs.

3. Fractionally-rated devices that are connected in series must be able to share the full line voltage during both steady-state and in transients. While complex gate drive circuits have been commercially utilized to provide gate-charge control to ensure steady-state and dynamic voltage sharing, they come at the cost of

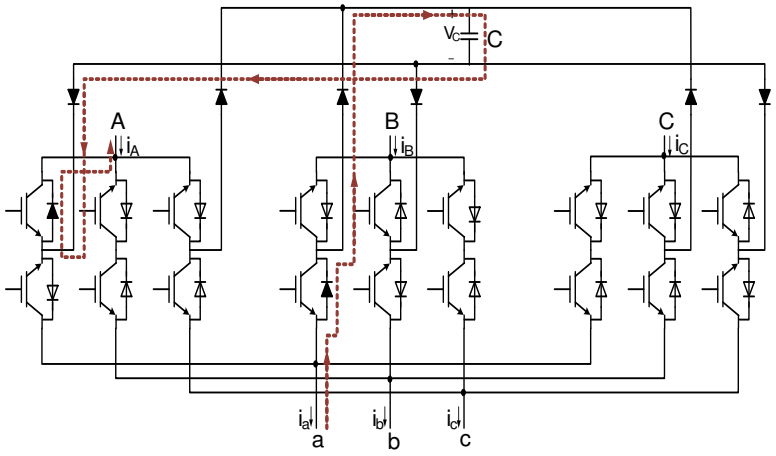


Figure 9.5: A snubber circuit for the matrix converter that leverages the anti-parallel diodes of the primary devices to provide paths to the snubber capacitor.

higher switching losses [63, 64, 6, 15, 33, 73]. Further, if high switching frequency is also desired when scaling up with smaller devices, gate-charge control becomes increasingly more difficult in managing the nanosecond time intervals. It would be more desirable for the snubber themselves to ensure voltages are shared equally among the devices. The snubbers of Figures 9.4 and 9.5 cannot provide this feature. While passive RDC snubbers have been examined for VSIs to provide voltage sharing, their operation is predicated upon existence of a DC voltage bus [5, 38]. Their effectiveness has not been evaluated for AC applications with a sinusoidal input voltage.

As a result of these limitations, direct AC and AC-AC converters have not been widely used in utility-grid applications, where high reliability, even under fault scenarios, is critically important. To address these limitations, a novel active AC snubber concept for the direct AC and AC-AC power converters is proposed with two different implementations. The concept and its implementations are validated through simulation results. Current-based commutation is assumed throughout this chapter in sequencing the AC switches.

9.4 Scaling with a Transformer

From a technical standpoint, the simplest way to scale a DVHC, and in particular the D-CAP, is to interface to the medium-voltage grid through a low frequency step-up transformer, as shown in Figure 9.6 for a boost D-CAP. Such an approach allows the D-CAP to be manufactured for low-voltage applications, where readily-available power devices can be utilized without resorting to series connecting the devices or employing multi-level topologies. This approach would simplify the design of the converter, as well as allowing a single modular design to target multiple markets, from the industrial sector to the utility, when interfaced with transformers of appropriate ratings. The total reactive power injected can then be scaled through paralleling of the modules.

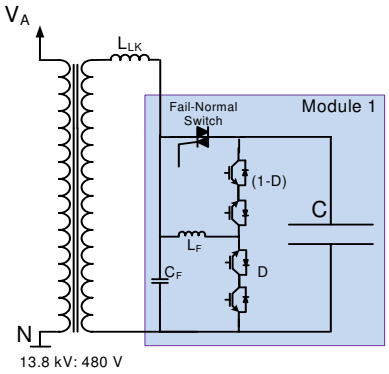


Figure 9.6: The 480 V boost D-CAP connected to the 13.8 kV line through a step-up transformer.

However, there are several limitations with this transformer-based approach to scaling:

1. The volumetric size and the footprint of the low-frequency transformer can be substantial. The size is inversely proportional to the frequency of the excitation. In locations with space constraints, especially in highly congested areas such as big cities, trying to acquire an adequate amount of real estate and then maneuver the transformer in place through tight spaces can be a real challenge.

2. The use of a low frequency transformer can increase capital, transportation, and installation costs. And depending on the location and project, can also impact the operation and maintenance costs. The relatively large size of low-frequency power transformers requires significant amount of high permeability silicon steel for its core and copper for its windings, both of which are relatively costly. Furthermore, there are the added costs of cabling, additional monitoring and protection equipment, thermal management system, civil engineering, concrete pad construction, etc.

3. Grid interfacing with a low-frequency transformer increases system losses and subsequently raises the variable operating costs.

4. As the power requirements increase, the current rating of the converter on the low-voltage side of the transformer increases as well, requiring thicker bus bars and larger devices, and necessitating paralleling of multiple modules. The current scaling can increase the cost of the system due to higher material requirements at a much faster rate than the voltage scaling.

Providing a direct-connect interface of the VAR and harmonic compensator to the medium-voltage grid is much more desirable. But even with the state-of-the-art techniques and power electronic technologies, it may be impractical to connect directly to the full range of medium-voltage levels, which is defined as 1 to 35 kV by ANSI/IEEE 1585 and IEEE STD 1623 standards. Above 13.8 kV, a hybrid solution may be more technically and economically viable, where the converter interfaces directly up to 13.8 kV and a transformer provides scaling beyond that point.

9.5 Approach 1: Series Connection of Devices

Series connecting the devices, like in Figure 9.7, is the most obvious way of realizing an equivalent switch of a higher rating from fractionally-rated devices. The operation

of the DVHCs with this approach is fundamentally the same as the low-voltage version, where all the switches on the top arm are commutated off a common switching command, and similarly, all the switches on the bottom arm are commutated based on a common signal that is complementary of the one supplied to the top. Subsequently, two-level voltages are synthesized across the output. A state machine implemented through field-programmable gate array (FPGA) or read-only memory (ROM) interprets these ideal duty pulses, and provides the actual commutation signal for each of the individual devices based on either current- or voltage-based commutation strategy.

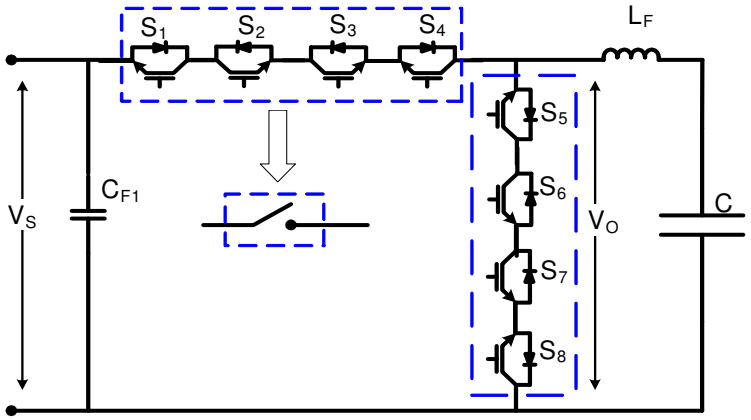


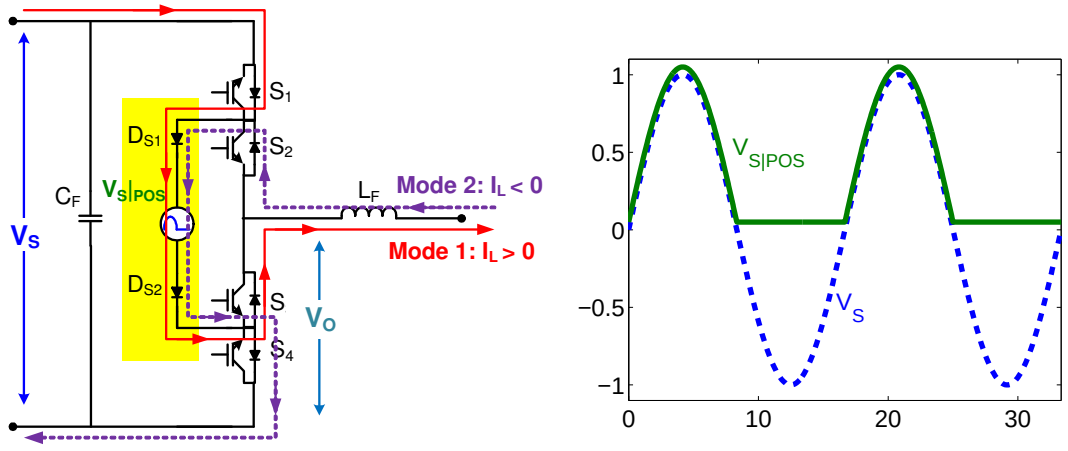
Figure 9.7: Series connection of devices with a lower rating to realize an equivalent bi-directional AC switch of a higher rating.

A major difficulty with a reliable implementation of this approach is in ensuring that each of the fractionally-rated devices block an equal share of the line voltage in order to not exceed their individual voltage rating. Historically, complex active gate-drives based on gate-charge control have been proposed to provide dynamic and stead-state voltage sharing. Gate-charge control is fundamentally based on controlling the device conductivity by actively regulating the flow of charge in and out of the gate such that each series-connected device presents the same effective impedance during both transient and in steady-state. However, by not driving the devices as hard as possible, the switching rise and fall times are lengthened, which subsequently

increases the switching losses. During steady-state, by not applying the maximum rated negative gate voltage to keep the device off, the leakage current increases, and in turn, the losses. While the latter losses may not be as significant, the increase in switching losses can be high. For grid applications, where losses translate to higher variable operating costs and a complex thermal management system, the converter needs to be as efficient as possible. Thus, an alternate, more efficient, approach is presented to provide the dynamic and steady-state voltage sharing.

9.5.1 Active AC Snubber

The concept of an active AC snubber is proposed for providing safe commutation, fault tolerance, spike-free snubber operation, and equal voltage sharing when integrated around series-connected devices. The snubber, drawn ideally and highlighted in Figure 9.8 in its most simplistic configuration, is shown integrated with a single-phase AC chopper cell comprised of two AC (bi-directional) switches in common-collector and common-emitter configurations. Arrangement of these two particular configurations of the AC switches in the manner shown is critical to providing a path for the snubbed energy to flow through the snubber circuit.



(a) Proposed snubber

(b) Snubber voltage

Figure 9.8: The proposed AC snubber integrated with a single-phase AC chopper cell.

The current paths through the snubber in both forward and reverse directions are highlighted. For instance, any time the current path is interrupted, and the inductor current is positive (mode 1), the "free-wheeling" path is through the diodes, D_1, which is the diode of device S_1, and D_{S1}, then through the actively regulated snubber with voltage, $V_{S|POS}$, and the diodes, D_{S2} and D_3, and finally back out through the filter inductor, L_F. If the inductor current is negative (mode 2), the "free-wheeling" path is through the filter inductor, L_F, the diodes, D_2, which is the diode of the switch S_2, and D_{S1}, through the regulated snubber with voltage, $V_{S|POS}$, and finally out the diodes, D_{S2} and D_4.

When the converter is nominally switching from the top to the bottom arm and vice versa, the voltage imposed across the output, V_O, is either the input voltage, V_S, or 0. Under the circumstances that an incorrect commutation sequence occurs and the current path suddenly becomes open through the main devices, the voltage imposed across the output when the energy in the filter inductor is snubbed is:

$$V_O = \begin{cases} V_S - V_{S|POS} \approx 0 & \text{for mode 1 and } V_S > 0, \\ V_S - V_{S|POS} \approx V_S & \text{for mode 1 and } V_S < 0, \\ V_{S|POS} \approx V_S & \text{for mode 2 and } V_S > 0, \\ V_{S|POS} \approx 0 & \text{for mode 2 and } V_S < 0. \end{cases} \tag{9.1}$$

Therefore, by regulating the snubber voltage appropriately, the voltage spike on the output due to snubber operation is eliminated almost entirely, thereby improving the THD of the converter as well as ensuring that volt-second balance across the output filter is well maintained.

The regulated voltage for the proposed snubber is the envelope of the voltage blocked by the main devices. In the single-phase AC chopper example, the regulated voltage is a half-wave rectified line voltage that is maintained slightly higher than the line voltage through a small DC offset. The offset reverse biases the diodes, D_{S1}

and D_{S2}, such that the snubber circuit is not needlessly drawing energy from the line. Because the snubber does not carry continuous duty current, its power rating is relatively small compared to the main devices and can potentially be integrated as part of the gate driver itself.

When scaling a converter through series connection of the devices, the snubber can be applied around each power switch as shown in Figure 9.9, and through the regulated snubber voltages, ensure equal voltage sharing among the devices. In this particular example, four series-connected devices constitute an AC power electronics building block (AC PEBB). The voltage across each snubber within the AC PEBB is regulated to either half the positive half-cycle of the input voltage, $V_{S/2|POS}$, or half the negative half-cycle of the input voltage, $V_{S/2|NEG}$, depending on the orientation of the main devices that they are connected across. As more devices are connected in series, the snubber voltages are scaled accordingly, relative to the line voltage.

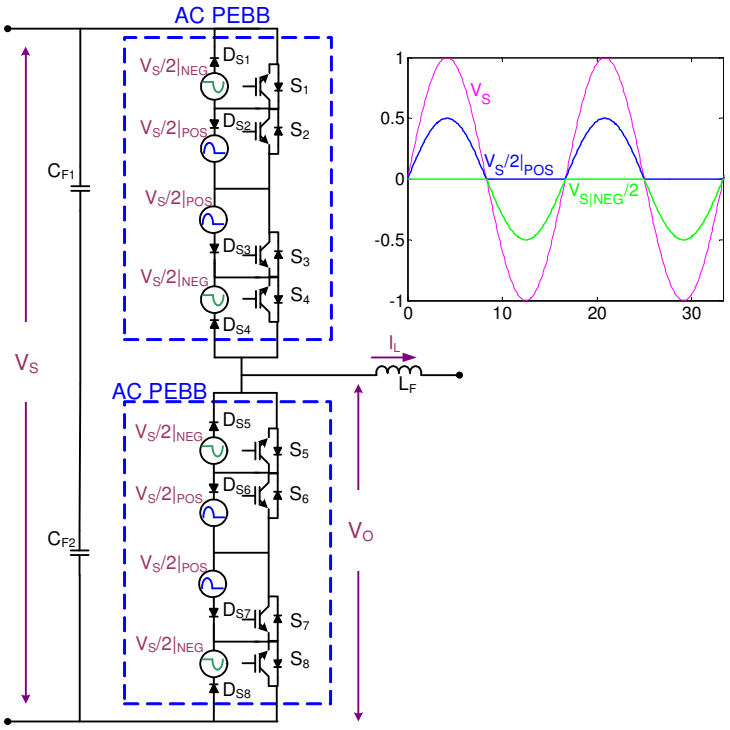
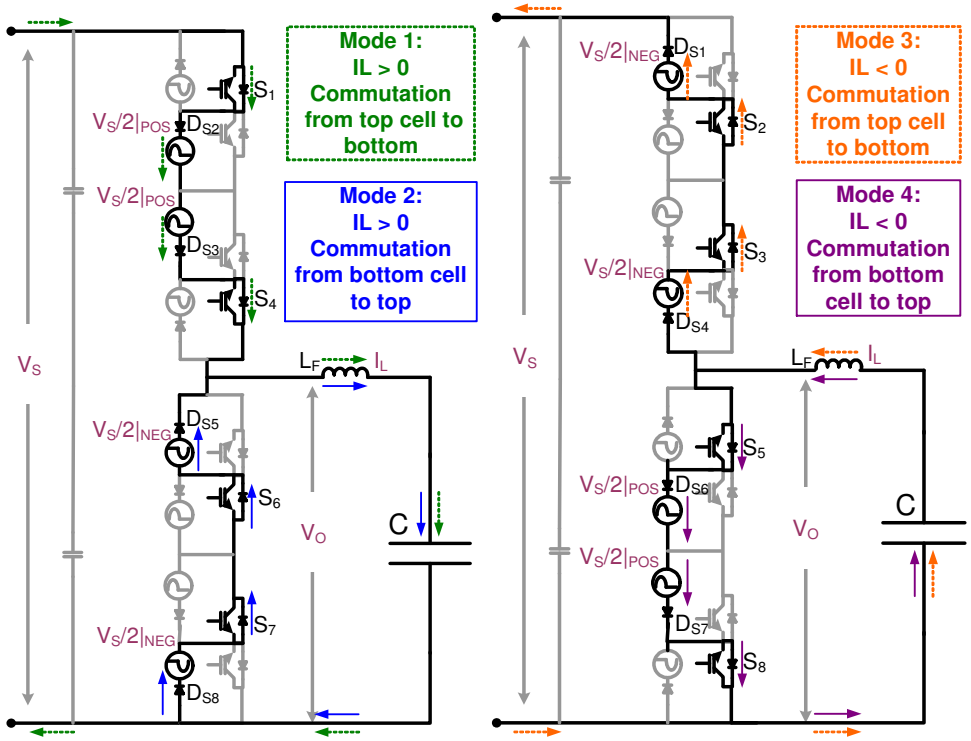


Figure 9.9: The snubbers are integrated around each primary device to ensure equal voltage sharing when series-connecting the devices.

The four modes of operation when the snubbers are operating are shown in Figure 9.10. For any given voltage or current polarity, when the established current path is suddenly interrupted, there are always alternate paths for the trapped energy to flow through. Due to these safe commutation and fault tolerance features, as direct AC converters are applied to grid applications, reliability of the converter and the system it is supporting remains high.



(a) Modes 1 and 2

(b) Modes 3 and 4

Figure 9.10: The four modes of converter operation when the AC snubbers are activated.

The voltage imposed across the output during the four modes of snubber operations are:

$$V_O = \begin{cases} V_S - 2\frac{V_S}{2}|_{POS} \approx 0 & \text{for mode 1 and } V_S > 0, \\ V_S - 2\frac{V_S}{2}|_{POS} \approx V_S & \text{for mode 1 and } V_S < 0, \\ 2\frac{V_S}{2}|_{NEG} \approx 0 & \text{for mode 2 and } V_S > 0, \\ 2\frac{V_S}{2}|_{NEG} \approx V_S & \text{for mode 2 and } V_S < 0, \\ V_S - 2\frac{V_S}{2}|_{NEG} \approx V_S & \text{for mode 3 and } V_S > 0, \\ V_S - 2\frac{V_S}{2}|_{NEG} \approx 0 & \text{for mode 3 and } V_S < 0, \\ 2\frac{V_S}{2}|_{POS} \approx V_S & \text{for mode 4 and } V_S > 0, \\ 2\frac{V_S}{2}|_{POS} \approx 0 & \text{for mode 4 and } V_S < 0. \end{cases} \tag{9.2}$$

So, once again there are no voltage spikes that are outside the envelope of the input voltage waveform when the snubbers are operating.

In summary, the following features are made possible via the utilization of the proposed active AC snubber:

1. Safe commutation of the devices, even with utilization of sensors of low quality and with various delays/errors in the controller and gate drives.

2. Fault tolerance, where should the devices be suddenly turned off due to a fault within or external to the converter, the energy in the filters and parasitics of the converter can be safely sunk into the snubber to be stored for future use or dissipated appropriately without causing catastrophic failure of the main devices.

3. Wave-shaped snubber voltage ensures spike-free snubber operation.

4. When applied to scaling, the snubber ensures equal voltage sharing among the series-connected devices.

9.5.2 Implementation 1: Low-Frequency Rectification

The first implementation of the proposed active AC snubber concept is shown in Figure 9.11. A low-frequency transformer is used to provide energy transfer between the line (the grid) and the snubber capacitors, C_{S1} and C_{S2}. The transformer's turn ratios are appropriately set to control the voltage across the snubber capacitors to be slightly higher than the actual blocking voltage of the main devices. This is done to reverse bias the snubber diodes, D_{S1} and D_{S2}.

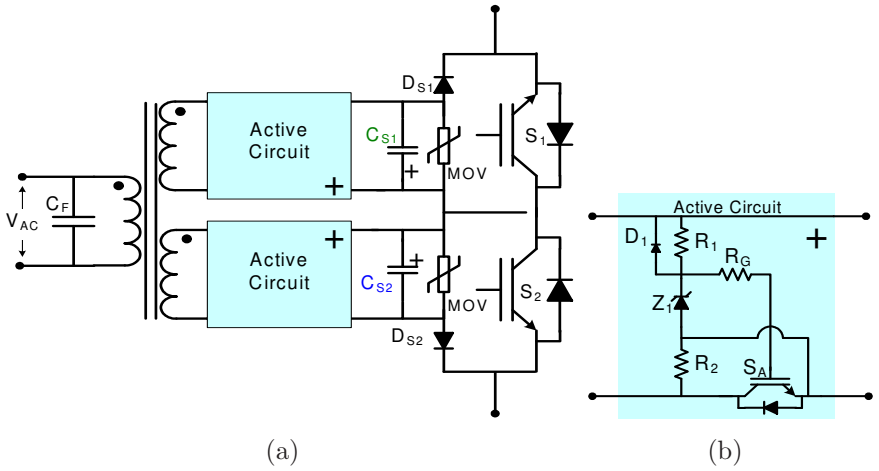


Figure 9.11: The AC snubber implemented using a low-frequency transformer to transfer energy between the line and snubber where half-wave rectification is controlled using a single transistor.

The half-wave rectification is achieved through the "Active Circuit" shown in the figure, where the switch, S_A, typically implemented with an IGBT and an anti-parallel diode, is automatically activated when the line voltage forward biases the diode. When a snubber capacitor, C_{Sx}, is charged from zero to peak of the line voltage, the charging current flows through this anti-parallel diode.

As the anti-parallel diode becomes forward biased, the components R_1, R_G, and Z_1 drive the snubber IGBT to turn on, thereby preparing the switch to conduct the current in reverse direction when the snubber capacitor voltage starts decreasing back down to zero. The components, D_1, R_2, R_G, and forward drop of Z_1, facilitate

in turning the IGBT off when the transformer secondary voltage becomes negative. Therefore, during the negative cycle, the snubber capacitor is negatively charged to the sum of forward drops of the zener and the diode, D_1.

The resistor, R_1, biases the zener, Z_1, to develop its reference voltage during the positive half-wave of the transformer secondary voltage.

When the AC snubber is connected according to the polarity marker, voltage across the snubber capacitor, C_{S2}, is a positive half-wave rectified voltage, while the other capacitors, C_{S1}, experience a negative half-wave rectified voltage.

In order to dissipate large amount of energy very quickly during fault contingencies when the main devices are suddenly turned off, an MOV is typically placed in parallel with the snubber capacitor. The MOV clamps the capacitor voltage within a certain level and dissipates the excess energy, protecting both the main devices and the snubber circuitry. Additionally, anti-series-connected zeners may be employed in parallel with the MOV to improve the response time of the voltage clamping mechanism.

This implementation requires the transformer to be connected to an even number of snubbers, where half the snubbers operate off the positive half-wave and the other half operate off the negative half-wave, to prevent a DC bias on the transformer.

9.5.2.1 Validation of Implementation 1 through Simulation

To demonstrate the concept, the snubber circuit of Figure 9.11 is applied to the circuit shown in Figure 9.9 and simulated. The input line voltage is 1600 V peak, thus each of the main IGBTs/diodes block 800V peak. The load is comprised of series-connected RLC components with R = 1 Ω, L = 200 μH, and C = 350 μF. Real device models for the main IGBTs and diodes are utilized and simulated in Synopsys Saber. The snubber capacitors, C_{Sx}, are sized to be 0.16 μF. The results are given in Figure 9.12.

The inductor current contains a significant amount of switching harmonics, which makes determining the polarity very difficult around the zero crossings. In turn, the

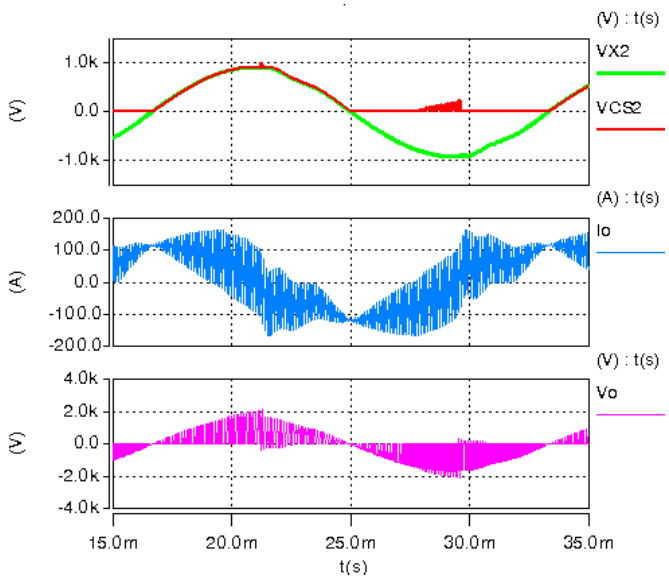


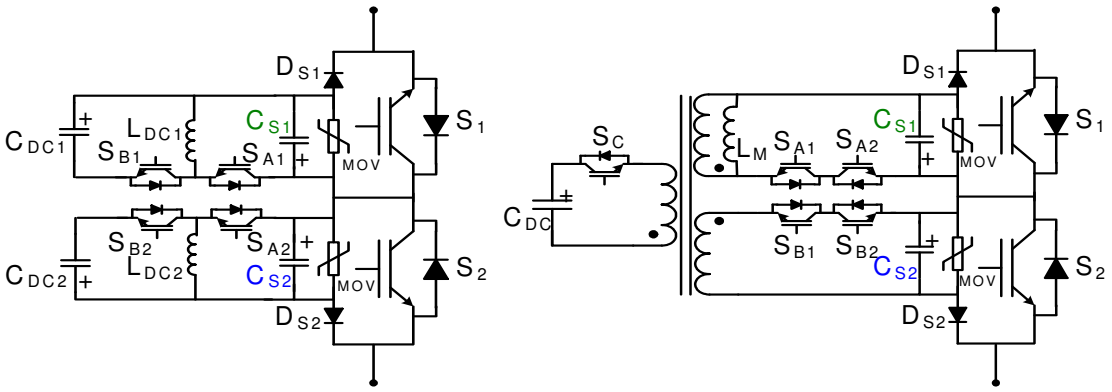
Figure 9.12: The voltage across the snubber capacitor, VCS2, the input voltage to the snubber circuit and the secondary of the transformer, VX2, the load current, Io, and chopped up voltage across the output, Vo

snubber capacitor experiences repeated voltage excursions during the zero crossings of the current due to the snubbed energy, as shown in the top plot. But because the snubber voltage is well regulated, the output spikes from the snubber operation are mitigated.

9.5.3 Implementation 2: High-Frequency Synthesis

The second implementation of the AC snubber is shown in Figure 9.13(a), which is based on the buck-boost DC-DC converter topology, where the converter synthesizes the half-wave rectified voltage across the main snubber capacitors, C_{Sx}, while the DC capacitors, C_{DCx}, serve as the energy tanks to provide the energy for synthesizing.

Unlike the low-frequency implementation, this implementation can actually be installed as a single unit and not necessarily in pairs, which makes this approach quite suitable for applications that only require a single or odd number of snubbers. Such requirements are quite typical in the numerous low-voltage industrial applications with voltages less than 480 V, where a single snubber can be configured similar to



(a) Buck-Boost (b) Flyback

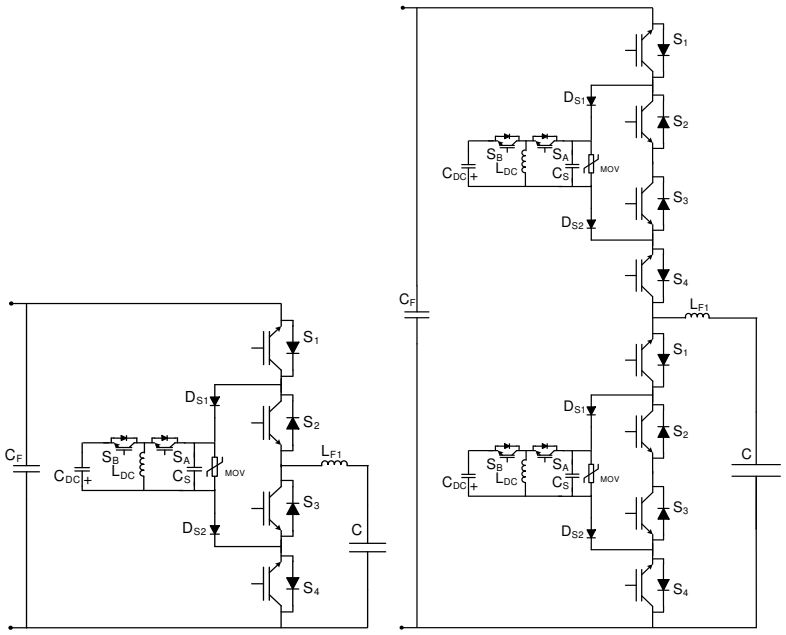
Figure 9.13: High-frequency approach of implementing the proposed AC snubber.

Figure 9.8.

An alternate converter integration of the snubbers is shown in Figure 9.14, where the snubbers provide safe commutation and fault tolerance but are not configured for voltage sharing. This configuration requires that an alternate means of ensuring equal voltage sharing is implemented. Here, only one AC snubber is used per arm: one on the top, one on the bottom. When scaling up further, one AC snubber is utilized for every two AC switches to maintain an alternate conduction path for the current.

A slightly alternate topology for this second implementation is depicted in Figure 9.13(b), where a single DC capacitor is used to synthesize voltage for two or more snubber capacitors through an isolated DC-DC flyback converter. While the active device count has gone up by one, the number of DC capacitors is reduced. The general operating principles remain essentially the same.

These two DC-DC-converter-based implementations can be integrated with the gate drive circuit. The snubber configuration is selected based on the number of devices driven by a single gate drive PCB. For example, if the PCB is driving a single AC switch (two IGBTs), then a flyback converter can couple a single DC capacitor to two snubber capacitors, as shown in Figure 9.13(b). However, if the PCB is driving



(a) Low-voltage (b) Medium-voltage

Figure 9.14: Simplified snubber utilization where the AC snubbers are providing safe commutations and fault tolerance but not voltage sharing.

a single IGBT instead, then the buck-boost configuration of Figure 9.13(a) is more appropriate.

While the two types of AC snubber implementations are very different, the objective remains the same: maintain a half-wave rectified voltage of the line voltage across the snubber capacitors, scaled based on the peak blocking voltage of the main IGBT with which the snubber is associated. If the IGBT blocks a non-sinusoidal or a DC voltage, the circuit synthesizes correspondingly similar envelope across the snubber capacitor as well, such that no spike is observed at the output when the snubbers operate. This makes the converter-based AC snubber very versatile in addressing a numerous different applications.

Both the buck-boost and flyback topologies operate in a discontinuous conduction mode (DCM), shuffling energy back and forth as required. This contributes to reduced switching losses as the beginning and the end of a switching cycle in DCM always

occur with a zero current. Managing parasitic resonances and losses are also simpler in DCM.

Since it is desirable to have a self-powering snubber circuit, the energy to drive the switches must ultimately be extracted from the energy stored in the snubber capacitors, C_{Sx}. As the line voltage goes through a full cycle, both the positive and the negative half-waves, the snubber capacitors are automatically charged to the peak of the line voltage through the snubber diodes, D_{Sx}. The energy is extracted from the snubber capacitors and is used to charge the DC capacitors. Once adequate amount of energy is stored in the DC capacitor, energy no longer has to be extracted from the line but can be shuffled back and forth between the DC capacitor and the snubber capacitor; at least until the tank has to be replenished due to the losses and the loading.

While ultimately the control power is drawn from the DC capacitor, as it provides a more stable voltage than the pulsating voltage across the snubber capacitor, the energy required during the initialization is drawn from the snubber capacitor, assuming the DC capacitor voltage is zero initially. To operate the control power in a dual source mode, a small relay (either electromechanical or solid-state) is used to switch between the snubber capacitor and the DC capacitor. Once the voltage across the DC capacitor is above a certain threshold, the relay switches position and changes the source from the snubber to the DC capacitor. This relay switching event also changes the mode from "initialization" where the primary objective is to charge up the DC capacitor, to "operational" where the circuit starts to synthesize a half-wave rectified voltage and the gate drive starts to drive the main IGBTs. The number of line cycles to go from initialization to operational mode depends on the size of the snubber and DC capacitors, and the device ratings that limit the speed at which the charges can be drawn.

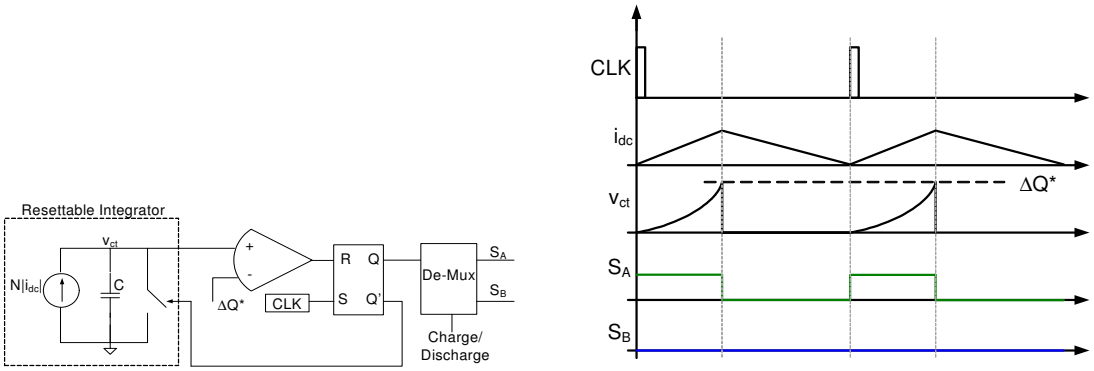
As the energy in the DC tank starts to deplete after multiple line cycles due to

losses in the power conversion within the snubber circuit, additional energy is pulled from the line.

Alternatively, as the snubbers are integrated on the gate drive board, the DC capacitors for the snubber can be the same as the DC supply for the gate drive board. Here, it is assumed that the DC power is supplied through alternate means and has the necessary BIL rating for operation at medium voltages. Combining the gate drive and snubber sources would then necessitate the use of the flyback topology for the required isolation.

9.5.3.1 Control of the High-Frequency AC Snubber

For simplicity, the control and operation of the high-frequency AC snubber is discussed using the buck-boost configuration. Charge-based control is utilized to charge and discharge the snubber capacitors. The control architecture is depicted in Figure 9.15.



(a) Schematic (b) Waveforms

Figure 9.15: Conceptualized controller schematic and the relevant waveforms for controlling the AC snubber.

The reference charge is calculated based on the relationship of charge to voltage in a capacitor, $Q = C\Delta V$, and energy stored in a capacitor, $E = \frac{1}{2}CV^2$. Therefore, the reference charge required to build or lower the voltage on the snubber capacitor,

C_S, is calculated by,

$$\Delta Q^* = \begin{cases} \frac{\hat{V}_{ref}+\hat{V}_{CS}}{2\hat{V}_{DC}} C_S \left|\Delta \hat{V}^*\right| & \text{when charging } C_S, \\ C_S \left|\Delta \hat{V}^*\right| + \Delta Q_L & \text{when discharging } C_S, \end{cases} \tag{9.3}$$

where

$$\begin{aligned} C_S &\equiv \text{snubber capacitance}, \\ \Delta \hat{V}^* &= \hat{V}_{ref} - \hat{V}_{CS} \equiv \text{desired voltage change}, \\ \hat{V}_{CS} &= \text{voltage across the snubber capacitor}, \\ \hat{V}_{DC} &= \text{DC voltage of the tank}. \end{aligned}$$

Additional charge reference, ΔQ_L, is included to compensate for the losses and loading of the DC capacitor through a non-linear proportional controller with the DC voltage as the feedback term. This controller is described by,

$$\Delta Q_L = K_P \hat{V}^2_{DC|err}, \tag{9.4}$$

where

$$\begin{aligned} K_P &= \frac{1}{2}\frac{C_{DC}}{V^*_{DC}} \equiv \text{proportional gain}, \\ \hat{V}_{DC|err} &= V^*_{DC} - \hat{V}_{DC}, \\ \hat{V}^*_{DC} &\equiv \text{reference DC voltage}. \end{aligned}$$

When energy is transferred from the snubber capacitor to the DC tank (discharge), the device, S_B, is kept off, and only the device, S_A, is modulated. When S_A is active, the inductor L_{DC} is charged. The current that flows during this time interval is integrated with respect to time. When the output of this integral equals the delta charge of Equation (9.3) for charging, the switch S_A is turned off using a Set/Reset logic chip, and the energy in the DC inductor is pumped into the DC capacitor. The

clock frequency is set such that the switch S_A is kept off until the current through the inductor drops to zero. The sequence is repeated in order to synthesize a voltage across the snubber capacitor according to some reference half-wave waveform, V_{ref}. The simple charge-based controller of Figure 9.15(a) provides fast dynamic response, excellent noise immunity, and elimination of distortion due to any higher-order effects as well as unaccounted resonances in the snubber circuit.

When energy is transferred from the DC tank to the snubber capacitor (charge), the process described above is reversed. This time, the device S_A is kept off, while the device S_B is modulated based on the charge reference given by Equation (9.3) for discharging.

The flyback topology operates based on the exact same principle. While additional devices are used in this topology, the switches S_{A2} and S_{B2} operate at the line frequency. When switches S_{A1}, S_{A2}, and S_C are operational over a certain half-cycle, the switches S_{B1} and S_{B2} are kept off to hold their corresponding snubber capacitor voltage to zero and prevent it from charging/discharging unnecessarily. Similarly, switches S_{A1} and S_{A2} are kept off when the switches S_{B1}, S_{B2}, and S_C are operating over the second half-cycle.

9.5.3.2 Validation of Implementation 2 through Simulation

The flyback topology of Figure 9.13(b) is simulated for the same operating conditions used in the validation of the low-frequency AC snubber implementation. While the conversion losses are present, the loading attributed to the snubber's and gate-drive's power supply is not modeled in order to minimize the complexity in this discussion. The components are selected as given by Table 9.1.

The results are shown in Figure 9.16. The charge-based controller is able to track the reference voltage quite closely when synthesizing the voltage across the

Table 9.1: The component values used for the simulation of the flyback-based AC snubber.

Component	Value		Description
C_{DC}	4.4	mF	DC energy tank
L_M	470	μH	Switching inductor
C_{S1}	0.16	μF	Snubber capacitor 1
C_{S2}	0.16	μF	Snubber capacitor 2
f_S	10	kHz	Switching frequency

two snubber capacitors. The snubber capacitor, C_{S1}, experiences a negative half-wave voltage, while the voltage across capacitor, C_{S2}, is a positive half-wave. The converter is operating in a DCM as inferable from the inductor current in the middle plot of Figure 9.16. Due to the conversion losses and without energy replenishment modeled in the simulation, the DC capacitor voltage is slowly decaying.

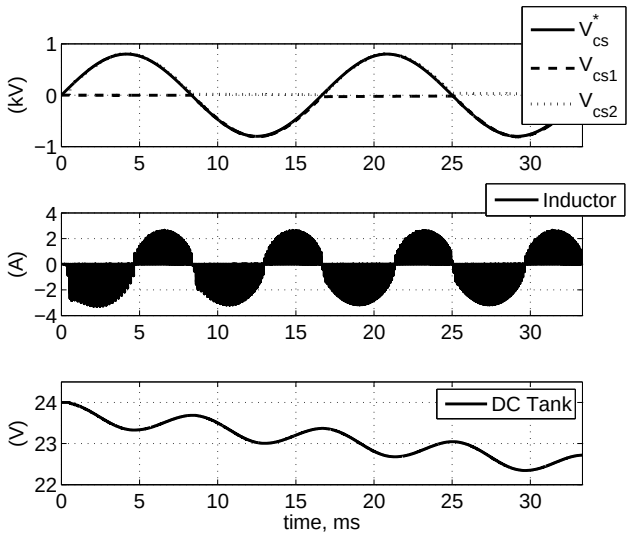


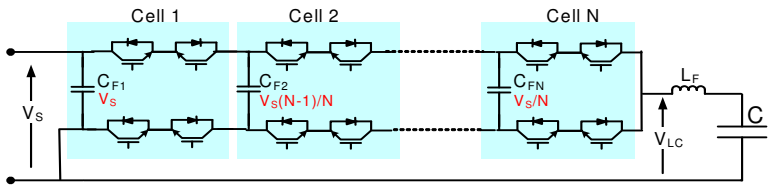
Figure 9.16: Simulation results of the flyback AC snubber without energy tank replenishment.

9.6 Approach 2: AC Flying Capacitor

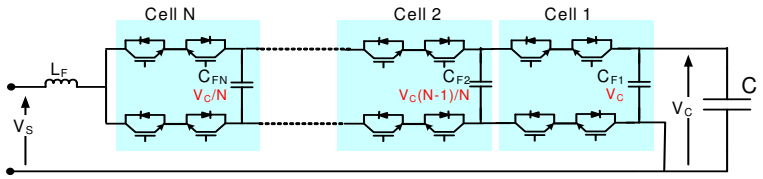
In extending the flying capacitor concept introduced for the VSIs to direct AC converters, an implementation was proposed for the matrix converter to reduce the required

voltage rating of the devices by half [78]. However, due to the polyphase nature of the matrix converter, the complexity in implementation and control involved in scaling increases significantly with each additional flying capacitor.

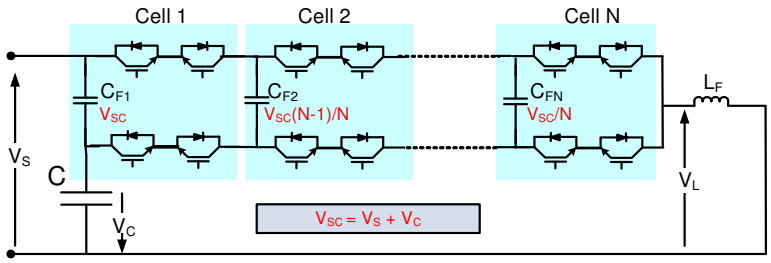
The flying capacitor concept has been applied to realizing a multi-level buck and boost configuration of the D-CAP for STATCOM applications in [22]. The N-cell circuits of these two topologies plus an additional one for the buck-boost, are depicted in Figure 9.17. The buck-boost circuit experiences a higher voltage rating equal to the line voltage plus the voltage across the main capacitor. Unlike a VSI, this is a direct AC topology and as such, it requires AC voltage regulation across the mid-point or "flying" capacitors, C_{F1} to C_{FN}, to ensure equal sharing of voltages among the switching devices.



(a) Buck



(b) Boost



(c) Buck-Boost

Figure 9.17: Multi-level D-CAP based on the concept of the flying capacitor multi-level VSI.

The topology is modularized based on cells, where each cell is comprised of four

IGBT devices and one AC capacitor. The voltage across each of the capacitors are regulated to:

$$V_{CFi} = V_{\Psi}\frac{N+1-i}{N}, \tag{9.5}$$

where

$$V_{\Psi} = \begin{cases} V_S & \text{for the buck,} \\ V_C & \text{for the boost,} \\ V_S + V_C & \text{for the buck-boost,} \end{cases}$$

$V_S \equiv$ Line voltage,

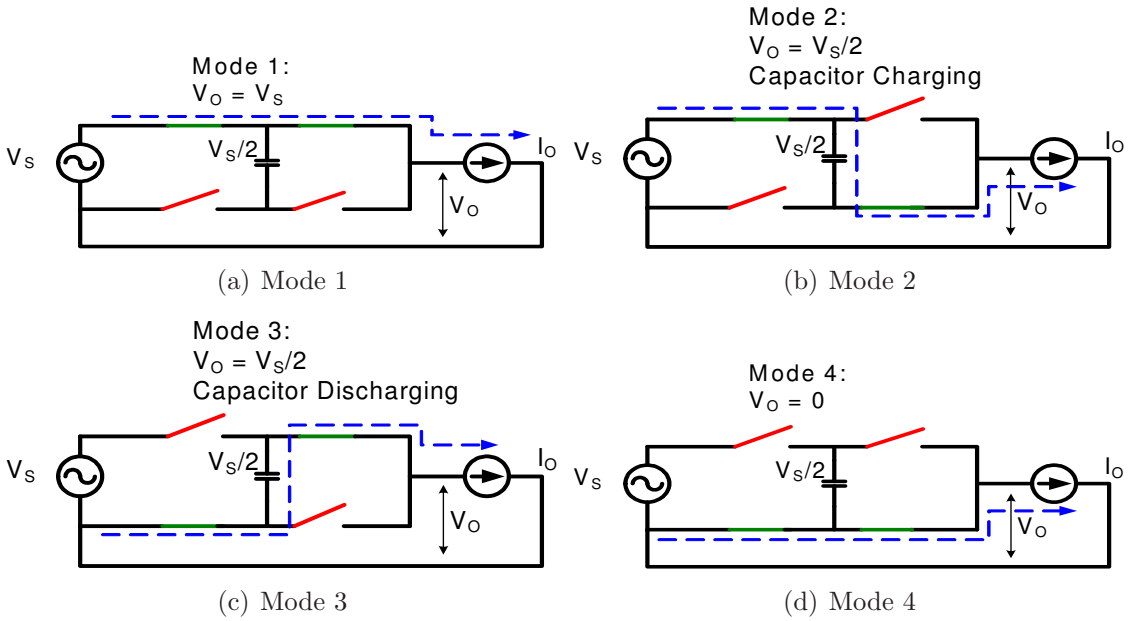
$V_C \equiv$ Voltage across the main capacitor, C,

$N \equiv$ Total number of cells,

$i = \{1, 2, 3, ..., N\} \equiv$ Cell designation.

The four modes of operation for the three-level ($N_{cell} = 2$) buck topology are given by Figure 9.18. The topology can potentially synthesize voltage with multiple levels across the filter inductor, while providing redundant states to charge and discharge the mid-point capacitor to regulate its voltage. However, the multi-level synthesis comes at the cost of larger mid-point capacitor(s) that also reduce the effective capacitance of the main capacitor due to the series injection.

An alternate approach is to consider the mid-point capacitor(s) as snubbers, and only utilize them to regulate the AC voltages for equal voltage sharing among the semiconductor devices, and not for synthesizing multi-level voltage across the output. This approach is simulated for a three-level topology, and the results are given by Figure 9.19. The output voltage swings between the envelope of the line voltage and zero, while the mid-point capacitor voltage is regulated to half that of the line voltage. But by eliminating the multi-level voltage synthesis, the dV/dt rating of



(a) Mode 1 (b) Mode 2

(c) Mode 3 (d) Mode 4

Figure 9.18: The four operating modes of the three-level AC-flying-capacitor-based buck D-CAP.

the passive components increase. Therefore, trade-offs are made depending on the approach taken.

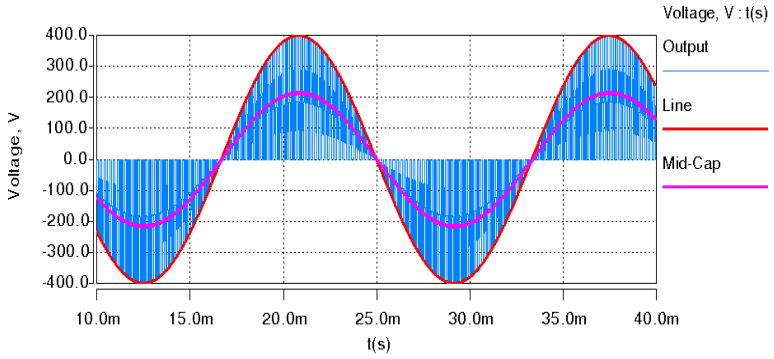


Figure 9.19: Simulation results of a three-level topology where the mid-point capacitor is maintained at half the line voltage and utilized only to provide equal voltage sharing such that the output experiences two-level synthesis.

A limitation in scaling to higher voltages with this topology is that while the voltage sharing among the switching devices occurs well enough, the voltage ratings of the mid-point capacitors increases linearly the closer the capacitor is to the line,

as given by Equation (9.5). Therefore, the flying capacitors cannot be packaged with the power switches as a module at a fixed rating as each capacitor must be rated for a different voltage.

In enabling safe commutation and fault tolerance with this implementation, the AC snubbers are configured across the series switches in the minimalistic manner depicted by Figure 9.14, where voltage sharing is not required from the AC snubbers.

9.6.1 Simulation Results

The single-phase, two-cell, flying-capacitor-based buck D-CAP, depicted in Figure 9.20 and with the component values and operating conditions summarized by Table 9.2, is simulated. Additional input filter elements, C_{BASE} and L_1, have been added to the D-CAP in order to improve the THD performance of the injected current by suppressing a greater amount of switching noise. A capacitor connected to an AC grid also injects reactive power, and as such, C_{BASE} also addresses the base reactive power requirements of the system/load and subsequently lowers the burden on the power devices by lowering their current ratings.

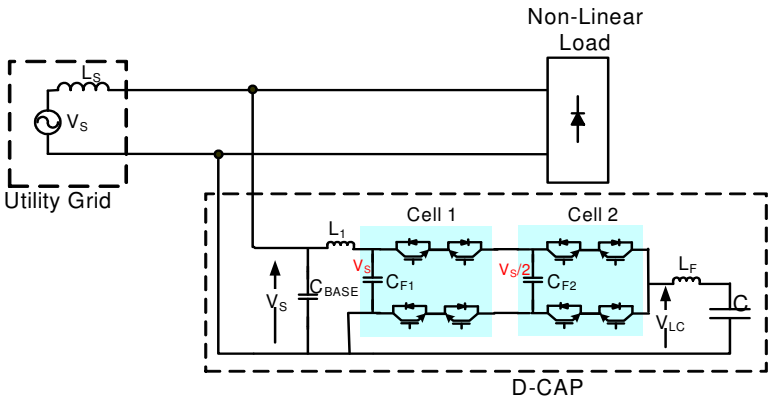


Figure 9.20: Schematic of the single-phase, two-cell, flying-capacitor-based buck D-CAP used in the simulation.

Figure 9.21 shows the voltage and current waveforms of the line, load, and the D-CAP over few line cycles. Figure 9.22 shows the voltages across each of the four

Table 9.2: The component values and the operating conditions selected for the simulation of the two-cell flying-capacitor-based buck D-CAP.

Operating Condition / Component	Value		Description
V_S	$2.4\sqrt{\frac{2}{3}}$	kV	Line voltage
L_S	100	μH	Line impedance
L_1	50	μH	Filter inductor
L_F	20	μH	Switching inductor
C	750	μF	Main capacitor
C_{F1}	50	μF	Cell 1 capacitor
C_{F2}	100	μF	Cell 2 capacitor
C_{BASE}	300	μF	Filter/base capacitor

AC switches in the D-CAP over five to six switching periods. And Figure 9.23 shows the fast Fourier transform (FFT) of the load and line currents.

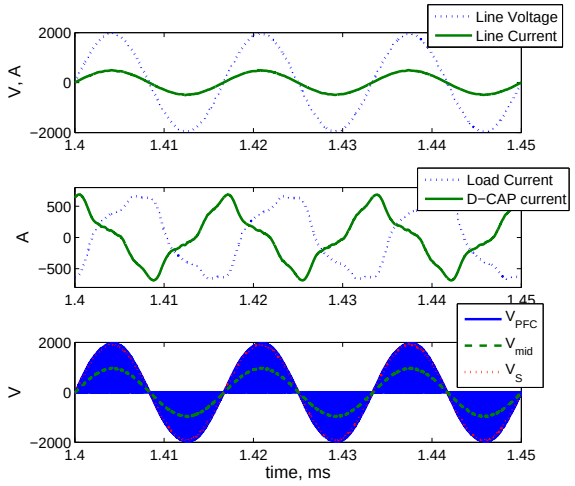


Figure 9.21: Time-domain waveforms of the line voltage and current (top), load current and D-CAP injected current (middle), and input voltage across the D-CAP, V_{DCAP}, the flying capacitor voltage, V_{mid}, and voltage across the "output" L_FC elements, V_{PFC} (bottom).

Even though the load current has substantial amount of harmonics, as indicated by the FFT plot, the D-CAP is able to suppress the harmonics from propagating

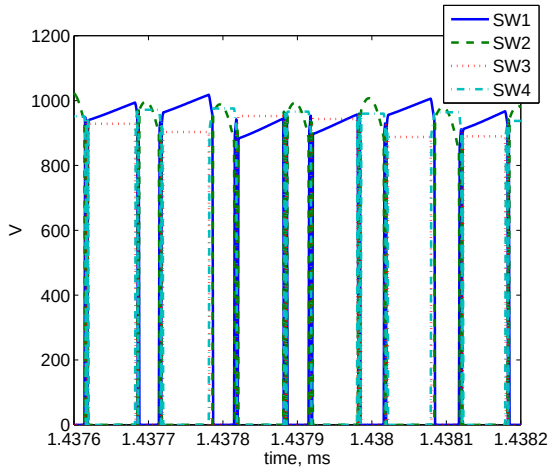


Figure 9.22: Voltages across each of the four AC switches.

into the grid. Furthermore, despite the load exhibiting poor power factor, the D-CAP is able to regulate the power factor to unity. The voltage across the flying capacitor, C_{F2}, is regulated to half the line voltage, which ensures that the voltage is shared equally between all the AC switches. The converter is controlled such that the flying capacitor, C_{F2}, is not used for synthesizing multi-level voltages. Therefore, the voltage across the output LC components is seen switching between 0 and the line voltage, V_S.

9.7 Approach 3: Cascaded Cells

The third approach to scale the DVHC to higher voltages is to cascade N two-level cells, such that each cell is only rated for V_S/N voltage, where V_S is the line-to-neutral voltage of the AC grid, as depicted in Figure 9.24 for the buck, boost and buck-boost configurations of the D-CAP. The approach is similar to the cascaded approach for the VSI where the full-bridge cells are replaced with the AC chopper cells.

Each cell or modules are designed to provide a fixed amount of reactive power at a given voltage. By cascading or series stacking the cells as shown, both the voltage rating of the DVHC system and the total power injected increases by a factor equal

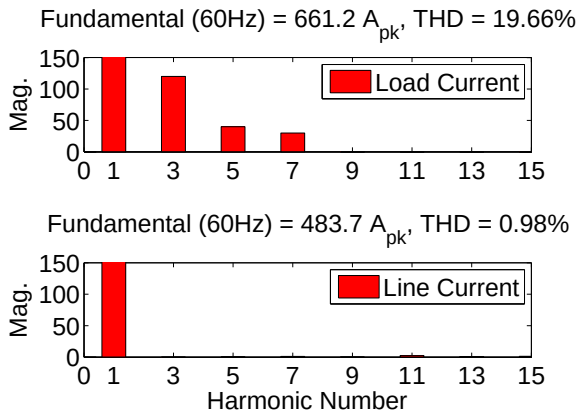


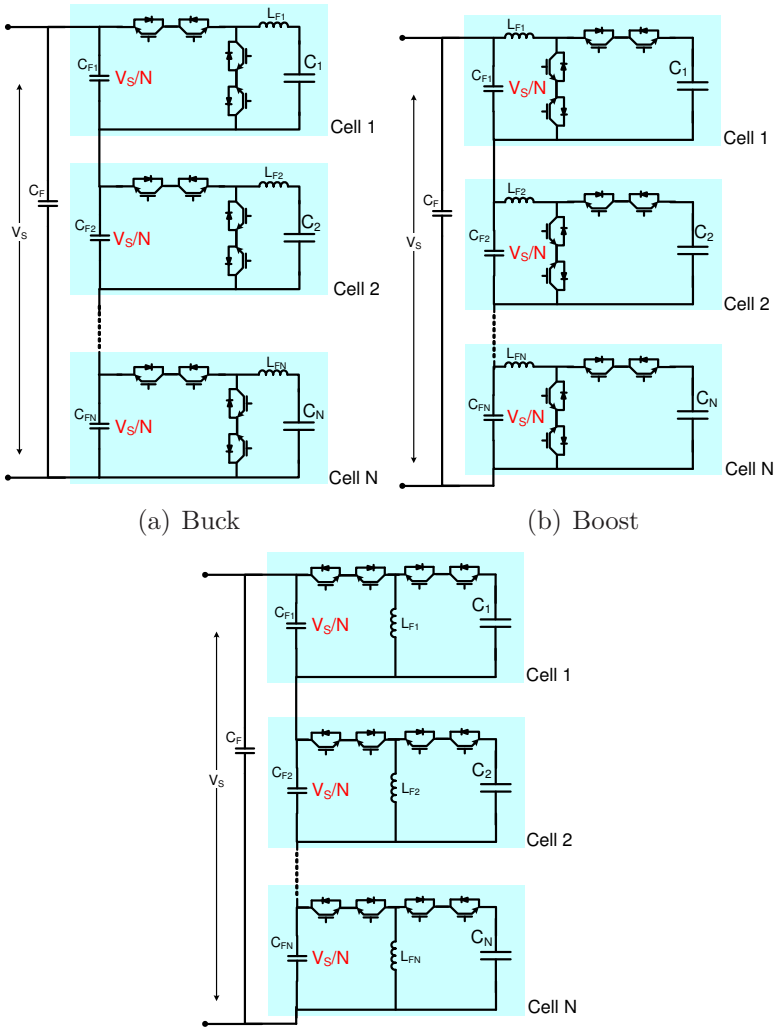
Figure 9.23: FFT of the load current (top), and the grid or source current (bottom).

to the number of modules. Increase in reactive power without scaling the voltage is realized through paralleling of the modules.

The cascaded multi-level D-CAP does not require an auxiliary circuit for ensuring that the AC voltages are shared equally among each of the cells in the topology. This is because each cell is essentially a variable capacitor and the voltage division occurs based on the effective impedance across each cell.

The effective impedance of each cell is varied based on duty-cycle control. Neglecting parasitics and higher order effects, the simplified expressions for the effective capacitance, C_{EFF}, of each cell controlled with only a constant duty cycle, K_0, are given for the three configurations by,

$$C_{EFF} = \begin{cases} C \cdot D^2 & \text{for the buck,} \\ C/\left(1-D\right)^2 & \text{for the boost,} \\ C \cdot D^2/\left(1-D\right)^2 & \text{for the buck-boost,} \end{cases}$$



(a) Buck (b) Boost

(c) Buck-Boost

Figure 9.24: Scaling the D-CAP by cascading modularized cells.

where

$$D = K_0 \equiv \text{Duty of the D-CAP},$$

$$C \equiv \text{Value of the main capacitor},$$

$$C_{EFF} \equiv \text{Effective capacitance as seen from the grid side.}$$

The effective reactance seen from the grid side is then,

$$X_{EFF} = \frac{1}{\omega C_{EFF}}.$$

With the same duty cycles driving the cells, each cell will see about the same voltage across its terminals. However, differences in the values of the passive elements in each cell due to manufacturing tolerances, as well as errors in monitoring and control circuitries are inevitable. The tolerances and errors can negatively impact the voltage sharing among the cells. These differences can be compensated through a feedback control. By introducing an additional voltage equalizing term, k_{CELL-i}, in the duty-cycle equation,

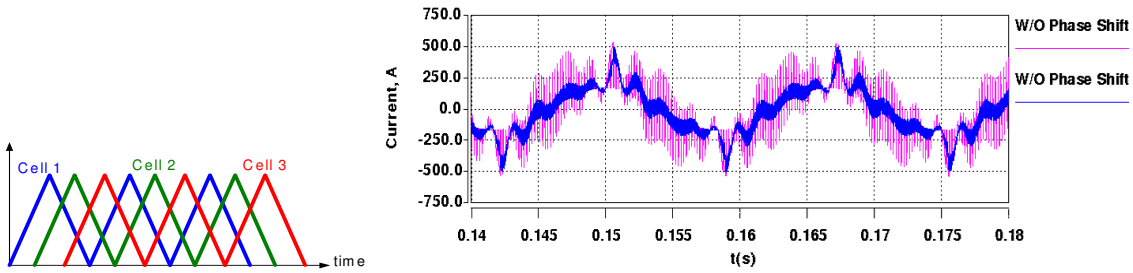
$$d(t) = K_0 + k_{CELL-i} + K_2 \sin(2\omega t + \phi_2) + K_4 \sin(4\omega t + \phi_4) + \cdots,$$

and closing the loop via feedback, the voltage differences can be compensated.

To minimize switching losses, it is often necessary to reduce the switching frequency, especially as voltage and power levels are scaled up. But, reduction in switching frequency leads to a higher level of switching harmonics, requiring larger and costlier filters. Phase-shifting the carrier waveform of each cell by $360/N$ degrees, where N is the number of cells, the switching harmonics can be significantly reduced.

For example, with three cells, the carrier waveform of each cell is phase-shifted by 120 degree, as depicted in Figure 9.25(a). The impact of carrier phase-shifting on the THD of the current injected by the D-CAP is significant, as depicted by Figure 9.25(b), where the D-CAP is operating with a switching frequency of 5 kHz and providing harmonic filtering for up to the eleventh harmonic. The current corresponding to carrier phase-shifted model has a significantly reduced switching harmonics. The harmonics can be further minimized with the increase in the number of cells, N, in series-cascade. Therefore, as the D-CAP is scaled up in voltage and power, larger but slower devices can be utilized without compromising on the spectral specifications.

In enabling safe commutation and fault tolerance, AC snubbers with the buck-boost implementation and configured as depicted by Figure 9.14(a) are used within each cell.



(a) Phase-shifted carrier waveform

(b) Impact of carrier phase-shifting

Figure 9.25: Simulated waveforms depicting the current injected by the D-CAP with and without carrier phase-shifting at a switching frequency of 5 kHz for a buck-configured D-CAP with three cascaded cells.

9.7.1 Simulation Results

To validate the concept of scaling through cascading modular cells, the D-CAP system has been configured as shown in Figure 9.26 with the operating conditions and component values summarized by Table 9.3. Additional passive filter components have been applied across the terminals of each of the cells in order to improve the THD of the injected current by suppressing greater level of switching harmonics. The input side capacitors also serve to provide base VAR injection required by the load, which leads to reduced current rating of the power switches. The capacitances have been selected such that the same level of VARs are injected for the same line conditions as the flying capacitor simulation in Section 9.6.1. The capacitances of the individual capacitors have to be higher to provide the same level of VARs as the topology with a single capacitor rated at full line voltage. This is because the effective capacitance of the stack is reduced through the series connection.

Figure 9.27 shows the voltage and current waveforms of the line, load, and the D-CAP over a few line cycles. In the top plot, the line voltage and current are in phase with each other, demonstrating that the D-CAP is injecting adequate amount of VARs to improve the power factor to unity. The load having poor power factor

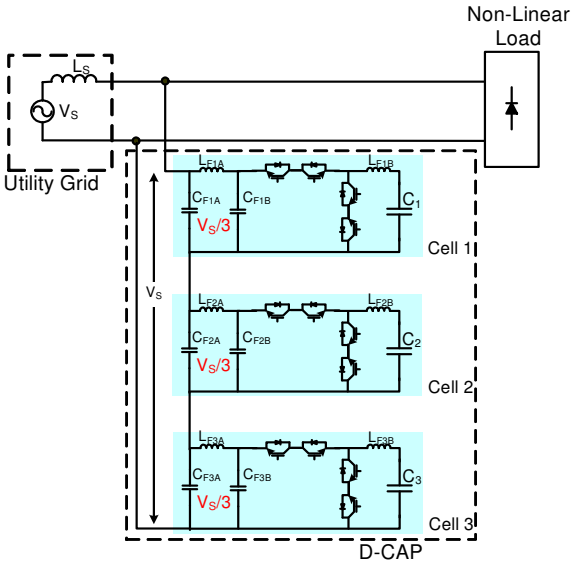


Figure 9.26: Simulated schematic of the single-phase, cascaded-cells buck D-CAP.

and THD is obvious from the middle plot, whereas the D-CAP current is in anti-phase with the harmonics of the load as well as containing adequate levels of leading VARs at the fundamental frequency to improve the power factor. The bottom plot demonstrates the voltages are equal across the terminals of each of the three cells.

Figure 9.28 shows the unfiltered synthesized voltage across the series connected components, L_{FiB} and C_i, over several switching periods. This figure clearly manifests the impact of carrier phase-shifting as the cell voltages are phase shifted by 120

Table 9.3: The selected component values and the operating conditions for the simulation of the three-cell cascaded-cells-based buck D-CAP.

Operating Condition / Component	Value		Description
V_S	$2.4\sqrt{\frac{2}{3}}$	kV	Peak line voltage
L_S	100	μH	Line impedance
L_{FiA}	16.67	μH	Filter inductor A for cell i
L_{FiB}	6.67	μH	Filter inductor B for cell i
C_i	2250	μF	Main capacitor for cell i
C_{FiA}	1200	μF	Filter capacitor A for cell i
C_{FiB}	300	μF	Filter capacitor B for cell i

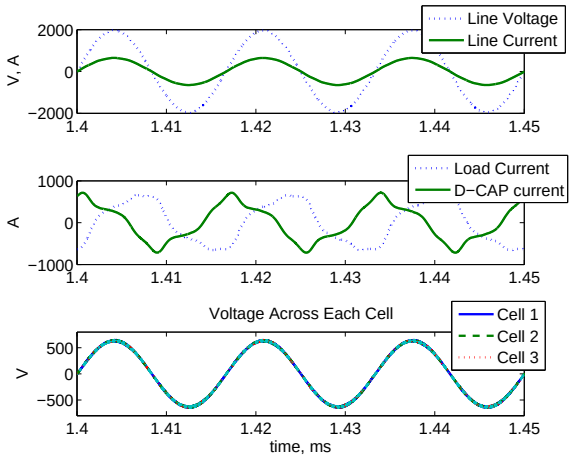


Figure 9.27: Time-domain waveforms of the line voltage and current (top), load current and D-CAP injected current (middle), and voltage across each of the three cells (bottom).

degrees. Furthermore, the peak voltage of each of the cells is equal to each other, validating that the voltages are shared equally among the three cells.

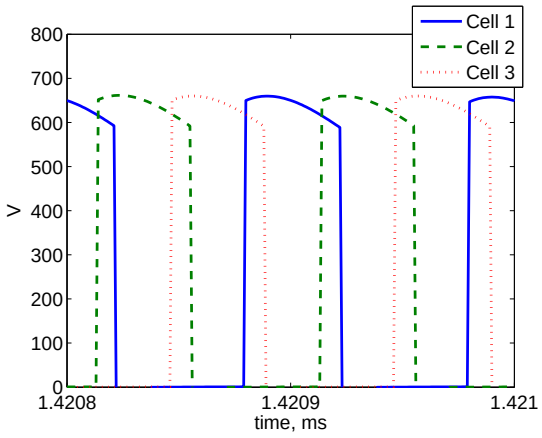


Figure 9.28: Chopped-up voltage across the LC components of each of the three cells.

Figure 9.23 shows the Fast Fourier transform (FFT) of the load and line currents, making it very clear that the line is free of all low-order harmonics. The D-CAP is effectively able to suppress the harmonics from propagating into the grid.

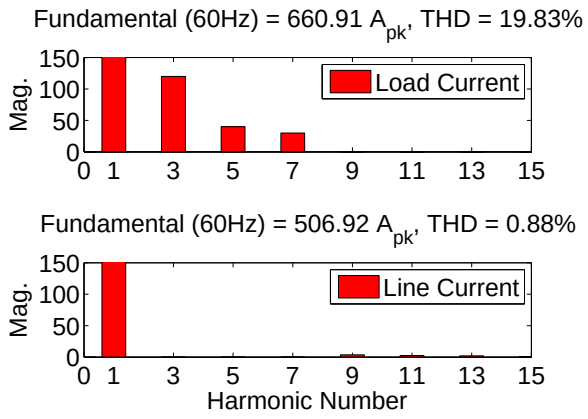


Figure 9.29: FFT of the load current (top), and the grid or source current (bottom).

9.8 Conclusions

Direct AC converters such as the D-CAP and direct AC-AC converters such as the matrix converter have some attractive salient features that include realization of silicon-rich topologies without bulk energy storage elements, which include large inductors or electrolytic capacitors. These features make these converters desirable for numerous applications that require high power density, long life, and high reliability.

However, applications for the matrix converter at medium voltages are limited, not only due to high device counts but also due to poor fault tolerance and lack of a reliable way to scale these converters to higher voltage levels. This is because there are no free-wheeling paths for the load and parasitic currents in cases where the devices are suddenly turned off or incorrectly sequenced. Safe switching with AC switches in direct AC and AC-AC converters mandate a complex switching pattern that is based on voltage and/or current polarity. Sequencing of the wrong commutation patterns due to incorrect assessment of polarity, especially around zero-crossings, can entirely disable the converter. Errors in measurements invariably exist but the design of the converter needs to be robust enough such that these errors do not degrade the performance or the life of the converter. Further, under a major fault, the switches

need to be turned off under local gate drive control. In an AC-AC converter, this can mean catastrophic failure of the converter unless appropriate snubbers and voltage clamps are used.

Scaling presents another challenge. As most grid-interfaced applications are at medium voltages, and lacking appropriately rated semiconductor switches to operate at higher voltage levels, an approach to scale up in voltages with fractionally rated devices is needed. One such an approach is through series-connection of the semiconductor devices. However, when series connecting AC (or bi-directional) switches, a mechanism is needed to ensure equal voltage sharing among the devices.

To address these various issues, a novel AC snubber concept has been presented in this chapter. The concept leverages the anti-parallel diodes of the main devices and provides an alternate path for energy to flow through, should the main devices suddenly turn off. The energy is sunk into a snubber capacitor with a regulated voltage. The voltage is regulated to a half-wave rectified sinusoidal voltage, mimicking the envelope of the blocking voltage of the main devices. Every time the snubber operates, no obvious spike is observed on the output, as is the case with the snubbers typically used with the matrix converters.

The AC snubber concept, in application with the DVHCs, ensures safe commutation even when there are errors in sensing, fault tolerance, especially lacking a free-wheeling mode for load current when devices are suddenly turned off, and provides equal voltage sharing when used around series-connected devices.

Two different AC snubber implementations are presented to wave-shape the snubber voltage and shuffle energy to and from the snubber capacitor. The first one is based on rectification of the scaled line voltage, where a single switch, comprised of an IGBT and its anti-parallel diode, provides rectification, while a low-frequency transformer provides scaling and isolation. In this implementation, energy is recycled directly with the AC line itself. The second type of implementation is based

on DC-DC converters operating with a charge-based controller that shuffles energy back and forth between the snubber capacitor and a DC capacitor or 'tank.' While the first implementation is the simplest, the converter-based implementation is more versatile, as it can be integrated with the gate drivers. The lack of a low-frequency transformer also enables smaller footprint and lowers the BIL requirements.

Three approaches for scaling the DVHC, and more specifically the D-CAP, to higher voltage levels are presented in this chapter. They are through series-connection of fractionally-rated devices, the AC flying capacitor, and cascaded cells. Each one is designed to be built using existing off-the-shelf devices with fractional ratings for operation at medium-voltages. Their operation and performance are validated through simulations.

The first approach, where fractionally-rated devices are series-connected, provides a compact means of scaling to higher voltages. However, since only the power switches are scaled, the passive components still have to be rated for high dI/dt and dV/dt associated with the switching of the full line voltage and current. To enable voltage sharing, fault tolerance, and safe commutation of the devices, the proposed AC snubbers are utilized around the devices and integrated with the gate drivers. This approach has the potential for the least amount of parasitics as the silicon devices and their modules can be packaged tightly, without any large filter components increasing the volumetric size of the modules. But as there are many novel concepts that have never been fully implemented, the difficulties in realizing a low-cost commercial design are not yet fully understood. These potential difficulties are in the implementation of the AC snubbers, controls system, and auxiliary circuits where inter-module operation, communications, and controls raise a unique set of challenges that have not been properly addressed with direct AC converters.

The AC flying-capacitor topology can synthesize multi-level voltages, significantly cutting down on the dV/dt rating of the passive components. The capacitors regulate

the voltages across the cell terminals, simplifying the controller complexity in ensuring voltages are shared equally among all the devices in both steady-state and during transitions in switching states. The dynamic voltage sharing feature is especially important as large amount of energy is being shuffled in and out of the devices by the gate driver, during which time the effective impedance across the devices are in flux. A disadvantage is that the approach requires capacitors of unequal ratings, making it difficult to build modular cells at a fixed rating. Further, as the number of cells increases, with only one switching pole per phase, the control complexity also increases dramatically as each of the flying capacitors have to be regulated holistically and with coordination.

The cascaded-cells approach provides a very modular means of scaling where all the cells are at a fixed rating. Scaling to high voltage or power is achieved by simply series cascading or paralleling the modular cells. Similar to the AC flying capacitor approach, the terminals of each cells are regulated at the line frequency, ensuring both steady-state and dynamic voltage sharing among the switching devices. The voltage sharing between the cells is realized through simple duty-cycle control. The disadvantage of this approach is that the sum total capacitance of all the capacitors are significantly higher for the same level of VAR injected at a nominal 1 pu voltage compared to the AC flying capacitor operated with the two-level switching. This is because the effective capacitance decreases with series connection of capacitors. Fortunately, the film-VAR capacitors are presently priced in terms of dollars per kVAR, and as such, the costs may not scale with capacitance as significantly.

All three are able to provide VAR and harmonic compensation quite effectively and with a good performance. They enable the DVHCs to be applied in a diverse number of markets, from residential and industrial applications with voltages less than 480 V, to utility-grid applications with voltages well above 10 kV.

CHAPTER X

DESIGN OF THE DYNAMIC CAPACITOR

10.1 Introduction

This chapter presents a set of generalized design equations in sizing and rating the various devices and components of the D-CAP, including the AC snubbers that are critical to the operation of direct AC converters. Based on these equations, three example designs of the D-CAP are discussed where the first design is for a low-voltage and the second and third for medium-voltage applications.

10.2 Design of the Power Stage

Realistic low-voltage implementations of the buck, boost, and buck-boost D-CAP with a third-order input filter are shown in Figure 10.1. The derivation of the design equations will be based on these three circuits. Since the functional cells for the medium-voltage topologies are also based on the same set of circuits, the design equations are equally applicable for sizing and rating the components of those topologies as well.

10.2.1 Selection of the Main Capacitor, C

The selection of the main capacitor, C, is based on the dynamic VAR requirements of the system and the selected topology with its corresponding operating domain. Based on the discretion of the designer, this last factor can significantly vary the sizing of the capacitor. For a nominal three-phase reactive power rating, Q, and with a base reactive power requirement of the system, Q_{BASE}, the main capacitor, C, for

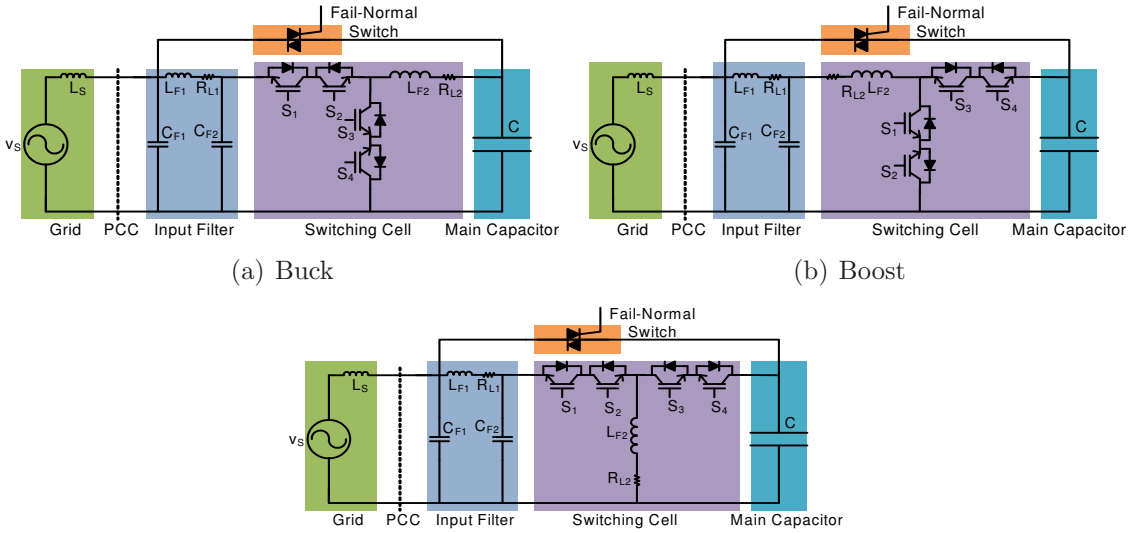


Figure 10.1: The three configurations of the D-CAP used in deriving the design equations.

the three configurations are sized as follows:

$$C = \begin{cases} \frac{1}{K_{0|NOM}^2} \frac{Q - Q_{BASE}}{3\omega V_S^2} & \text{for the buck,} \\ \left(1 - K_{0|NOM}\right)^2 \frac{Q - Q_{BASE}}{3\omega V_S^2} & \text{for the boost,} \\ \frac{\left(1 - K_{0|NOM}\right)^2}{K_{0|NOM}^2} \frac{Q - Q_{BASE}}{3\omega V_S^2} & \text{for the buck-boost,} \end{cases} \tag{10.1}$$

where

$$\omega \equiv \text{line frequency in rad/s,}$$

$$V_S \equiv \text{line-to-neutral grid voltage.}$$

These expressions are derived based on power balance between the input of the converter and the capacitor. The base reactive power, Q_{BASE}, which is the static reactive power required by the system, is subtracted in the derivation. This is because that requirement is fulfilled by the input filter capacitors, which also serve to suppress the switching harmonics. By removing the base requirements from the main capacitor, the rating of the active components and subsequently the cost of the system are reduced.

The value of the main capacitor depends on the nominal operating duty, $K_{0|NOM}$, where typical values are around 0.707, 0.2, and 0.5 for the buck, boost, and buck-boost topologies, respectively. A designer may select a different nominal operating point based on various trade-offs. In this design, it is assumed that under nominal grid conditions, $K_{0|NOM}$ provides the full rated power, Q. As the reactive power requirement of the system changes, the duty is varied from 0 to the nominal operating duty. The only time it is necessary to increase the duty past the nominal point is under sub-nominal grid voltages when 1 pu reactive current has to be maintained to support the grid. At which point, the duty can be increased up to $K_{0|MAX}$, when the losses start to severely stress the thermal management system.

In the design examples considered in this chapter, the upper limit on the duty cycles are set to 1, 0.33, and 0.6, for the buck, boost, and buck-boost, respectively, based on maximum allowable losses. The primary assumption here is that the sub-nominal grid voltages will occur for an indefinite amount of time on the system and by limiting the maximum duty, thermal meltdown can be prevented. However, clearly the assumption does not hold for fault-induced or fault-recovery events that last for only several line cycles, in which case, the maximum duty can be pushed higher. An optimal strategy is one that time-limits the duty cycle or one where the limit is based on thermal feedback.

As the harmonic compensation requirement emerges, a slight amount of even harmonic duty modulation can achieve harmonic filtering as well. Therefore, the nominal and maximum operating points are strongly dependent on both the electrical and thermal designs, as well as the electrical and the environmental operating conditions.

10.2.2 Selection of Inductor, L_{F2}

The filter inductor, L_{F2}, is sized to limit its current ripple within a certain value. The value of the filter inductor is estimated by combining the classical DC-DC converter

equations given by,

$$L_{F2} = \begin{cases} \frac{1}{f_s}\frac{(1-K_0)V_O}{2\Delta i_L} & \text{for the buck,} \\ \frac{1}{f_s}\frac{K_0 V_S}{2\Delta i_L} & \text{for the boost,} \\ \frac{1}{f_s}\frac{K_0 V_S}{2\Delta i_L} & \text{for the buck-booost,} \end{cases} \tag{10.2}$$

with the ideal converter gains,

$$V_O = \begin{cases} V_C = K_0 V_S & \text{for the buck,} \\ V_C = \frac{1}{1-K_0} V_S & \text{for the boost,} \\ V_C = \frac{K_0}{1-K_0} V_S & \text{for the buck-booost,} \end{cases} \tag{10.3}$$

and the current induced by a capacitor,

$$I_C = \omega C V_C, \tag{10.4}$$

to obtain the generalized equations as follows for the three configurations of the D-CAP:

$$L_{F2}C = \begin{cases} K_0|_{MAX}\frac{1}{f_s}\frac{1}{2\omega\gamma_I} & \text{for the buck,} \\ \left(K_0\left(1-K_0\right)^2\right)|_{MAX}\frac{1}{f_s}\frac{1}{2\omega\gamma_I} & \text{for the boost,} \\ \left(1-K_0\right)^2|_{MAX}\frac{1}{f_s}\frac{1}{2\omega\gamma_I} & \text{for the buck-booost,} \end{cases} \tag{10.5}$$

where

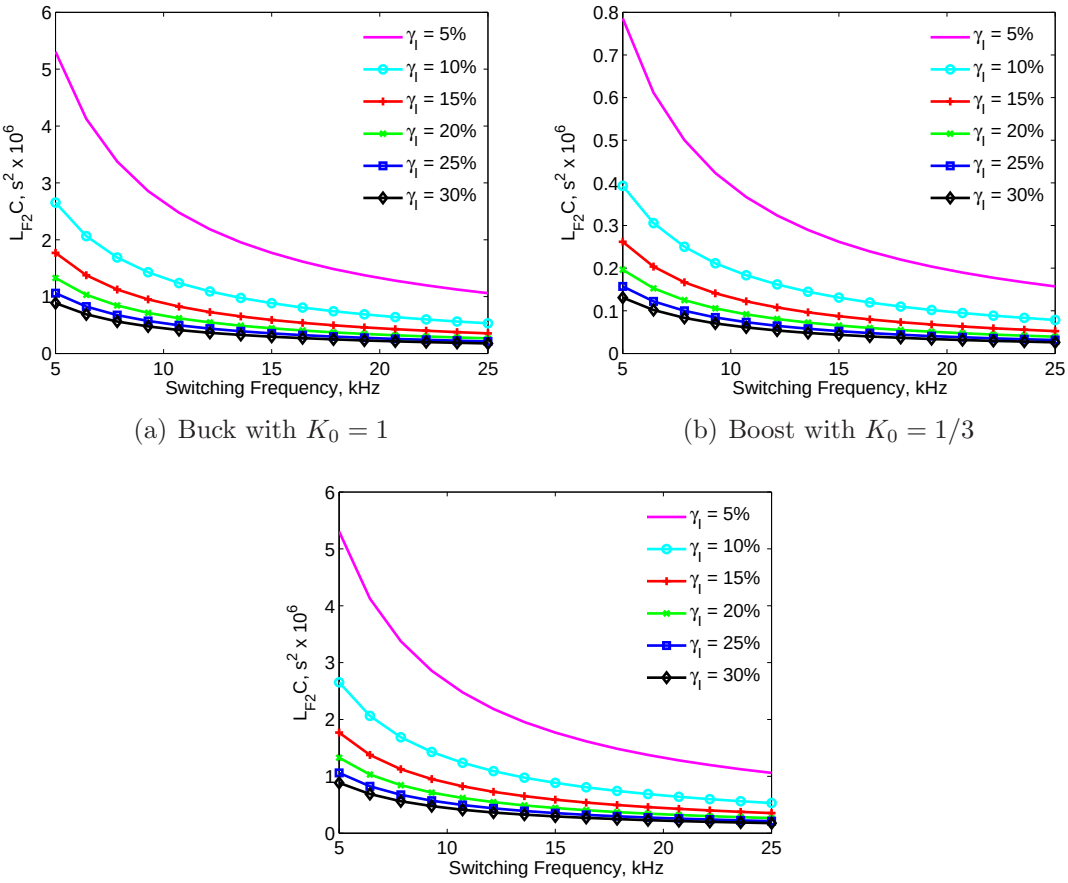
$f_S \equiv$ switching frequency (Hz),

$\gamma_I = \Delta i_L / I_{L|PK} \equiv$ ratio of peak current ripple to peak current.

The selection of the switching inductor is based on the desired current ripple, γ_I, and the three multipliers that are a function of the duty cycle, K_0. The duty cycle within the range, $[0, K_{0|MAX}]$, that maximizes the multiplier is used in sizing the inductor.

Once these two parameters are determined, the inductance is obtained by dividing by the value of the main capacitor, C.

With duty values of 1, 1/3, and 0 for the buck, boost, and buck-boost, which are the operating points that maximizes the filter requirements, the above expressions are plotted with respect to the switching frequency, f_S, for different values of the current ripple in Figure 10.2.



(a) Buck with $K_0 = 1$

(b) Boost with $K_0 = 1/3$

(c) Buck-Boost with $K_0 = 0$

Figure 10.2: Sizing the inductor, L_{F2}, with respect to the switching frequency for a range of current ripple.

The resistor, R_{L2}, depicted in the circuit diagrams is the parasitic resistance, represented in series with the inductor.

10.2.3 Selection of Input Capacitors, C_{F1} and C_{F2}

The sizing of the input capacitor, C_{F2}, for the three configurations are based on the ideal converter gains and the design equations of the classical DC-DC converter,

$$C_{F2} = \begin{cases} \frac{1}{f_S}\frac{(1-K_0)I_S}{2\Delta v_S} & \text{for the buck,} \\ \frac{1}{f_S}\frac{\Delta i_L}{8\Delta v_S} & \text{for the boost,} \\ \frac{1}{f_S}\frac{(1-K_0)I_S}{2\Delta v_S} & \text{for the buck-boost,} \end{cases} \tag{10.6}$$

to subsequently obtain the generalized expressions given by,

$$C_{F2}/C = \begin{cases} \left((1-K_0)\,K_0^2\right)|_{MAX}\frac{1}{f_s}\frac{\omega}{2\gamma_V} & \text{for the buck,} \\ \frac{K_0^2}{1-K_0}|_{MAX}\frac{1}{f_s}\frac{\omega}{2\gamma_V} & \text{for the buck-boost,} \end{cases} \tag{10.7}$$

and for the boost by,

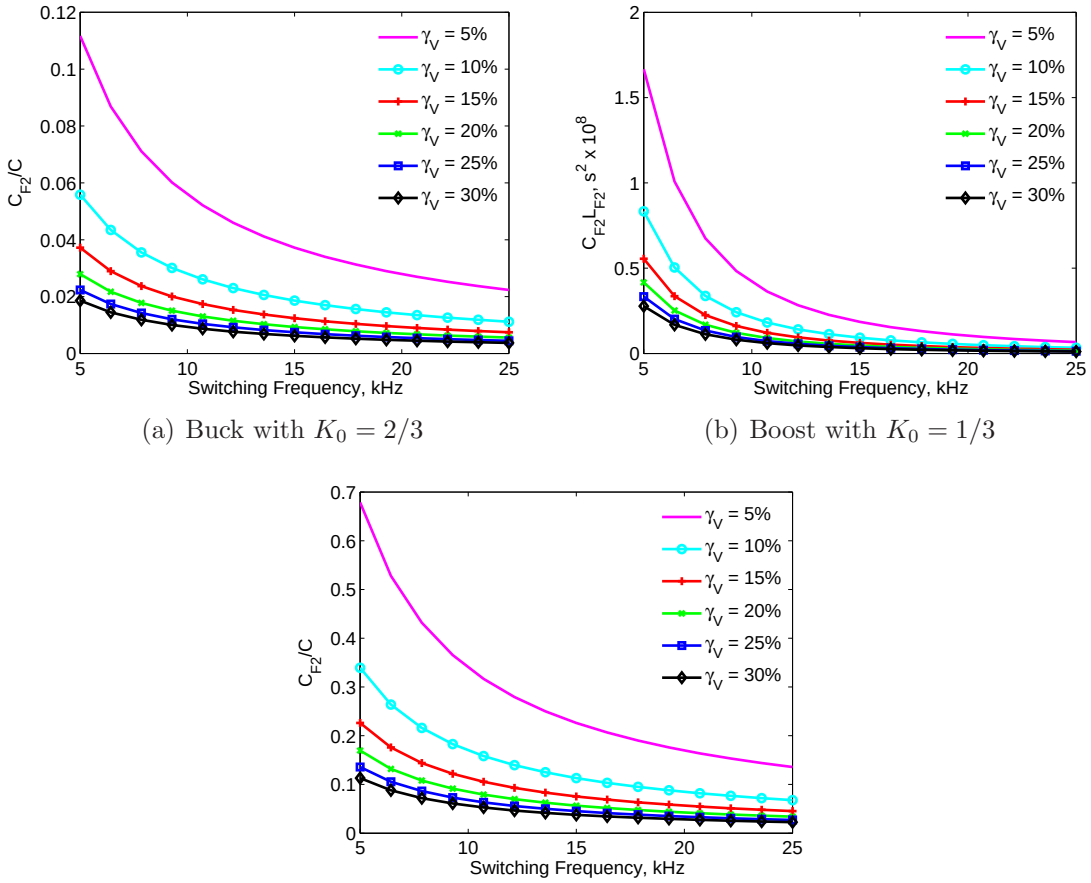
$$C_{F2}L_{F2} = K_0|_{MAX}\frac{1}{f_s^2}\frac{1}{16\gamma_V}, \tag{10.8}$$

where

$$\gamma_V = \Delta v_S/V_S \equiv \text{ratio of peak voltage ripple to peak line voltage,}$$

for a range of allowable voltage ripple, γ_V. Similar to the switching inductor, the input filter capacitors are selected based on the duty value, K_0, that maximizes the multipliers. For the buck and buck-boost configurations, C_{F2} is obtained by multiplying their respective expressions by the value of the main capacitor, C, while for the boost, C_{F2} is obtained by dividing by the value of the previously selected filter inductor, L_{F2}.

With the duty value of 2/3, 1/3, 3/5 for the buck, boost and buck-boost, the above expressions are plotted with respect to the switching frequency for different values of the voltage ripple in Figure 10.3.



(a) Buck with $K_0 = 2/3$

(b) Boost with $K_0 = 1/3$

(c) Buck-Boost with $K_0 = 3/5$

Figure 10.3: Derivations of the filter capacitor, C_{F2}, with respect to the switching frequency for a range of voltage ripple.

Although the capacitor, C_{F2}, is selected to suppress the switching harmonics, it also supplies reactive power. Therefore, the reactive power injected by the capacitors, C_{F1} and C_{F2}, is used to meet the base VAR requirements of the system or load. Their presence also reduces the overall burden on the converter by lowering the current rating of the devices and components, thereby reducing cost per kVAR of dynamic compensation. This is assuming that the filter inductor, L_{F1}, is not consuming significant amount of reactive power.

The capacitor, C_{F1}, is sized to provide the remaining base VAR requirements of

the system not already fulfilled by C_{F2}, as follows:

$$C_{F1} = \frac{Q_{BASE} - 3\omega V_S^2 C_{F2}}{3\omega V_S^2} \tag{10.9}$$

Here it is assumed that the three-phase capacitor, C_{F2}, has not met or exceeded the base requirements on its own, as the resulting value of C_{F1} would be negative. However, one may realize a design where the switching filter requirements do lead to excess base VAR injection by C_{F2}. In such a scenario, the value of the main capacitor, C, is reevaluated and trimmed smaller, while C_{F1} is set to a minimum value as required to decouple the filter, grid, and load inductors, or eliminated entirely if interactions are not an issue.

10.2.4 Selection of Input Inductor, L_{F1}

The filter inductor, L_{F1}, is sized to suppress the switching harmonics from penetrating the point of common coupling (PCC). Because C_{F1} is connected at the PCC and is sized to provide base VAR injection, it is assumed to be a voltage source. Then, the input filter stage, comprised of L_{F1} and C_{F2}, essentially becomes a second-order filter for suppressing the switching harmonics in the current. The transfer function for this second-order filter is given by:

$$H(s) = \frac{\omega_0^2}{s^2 + 2\alpha s + \omega_0^2},$$

where

$$\omega_0 = \frac{1}{\sqrt{L_{F1} C_{F2}}},$$
$$\alpha = \frac{R_{LF1}}{2L_{F1}}.$$

The value of L_{F1} is selected such that the harmonics at the switching frequency is attenuated by -20 dB. For a second-order filter, the filter gain drops by -40 dB/decade. By setting the 'knee' frequency, $\omega_k = \frac{2\pi}{\sqrt{10}} f_S$, where the gain starts to drop, the value

of L_{F1} is calculated:

$$L_{F1} = \frac{1}{\omega_k^2 C_{F2}}. \tag{10.10}$$

The knee point may have to be adjusted to account for the effects of damping.

10.2.5 Device and Component Ratings

In estimating the current and voltages of the semiconductor switches, the two-level configuration shown in Figure 10.1 is assumed but with the switches represented as ideal AC switches. Further, assuming that the fundamental component of the current greatly dominates the harmonic components, the devices and components are sized with constant duty operation. Voltage and current ratings are difficult to estimate under harmonic filtering applications, as the magnitude and phase of the harmonics are entirely load-dependent. Similar to inverter-based active filter designs, adequate safety margins should be given when rating the devices and components to account for harmonic compensation. A 200 percent overhead margin on the current and a 50 percent overhead margin on the voltage should be sufficient for most applications.

The voltage and current for the equivalent AC switch and the passive components are given by Table 10.1 and Table 10.2, respectively. Devices and components are rated based on these expressions and the added overhead margins to account for faults and harmonics.

Table 10.1: Estimated peak voltage, V_{SW}, and RMS current, I_{SW}, of the equivalent AC switches in the three configurations of the D-CAP.

Configuration	Voltage Rating (V_{PK})	Current Rating (I_{RMS})
Buck	$\sqrt{\frac{2}{3}} V_{LL}$	$\sqrt{\frac{1}{3}} \frac{Q}{V_{LL}} \frac{(1+\gamma_I)}{K_0}$
Boost	$\sqrt{\frac{2}{3}} V_{LL} \frac{1}{1-K_0}$	$\sqrt{\frac{1}{3}} \frac{Q}{V_{LL}} (1+\gamma_I)$
Buck-Boost	$\sqrt{\frac{2}{3}} V_{LL} \left(1 + \frac{K_0}{1-K_0}\right)$	$\sqrt{\frac{1}{3}} \frac{Q}{V_{LL}} \frac{(1+\gamma_I)}{K_0}$

In Table 10.2, the reactive power, Q_{CF1}, is the static VAR injected by C_{F1}.

Table 10.2: Estimated peak voltage and RMS current of the passive components.

Component	Configurations			
	Buck	Boost	Buck-Boost	Unit
C	V_S	$V_S \frac{1}{1-K_0}$	$V_S \frac{K_0}{1-K_0}$	V_{PK}
C_{F1}	V_S	V_S	V_S	V_{PK}
C_{F2}	$V_S(1+\gamma_V)$	$V_S(1+\gamma_V)$	$V_S(1+\gamma_V)$	V_{PK}
L_{F1}	$\frac{Q-Q_{CF1}}{\sqrt{3}V_{LL}}$	$\frac{Q-Q_{CF1}}{\sqrt{3}V_{LL}}$	$\frac{Q-Q_{CF1}}{\sqrt{3}V_{LL}}$	A_{RMS}
L_{F2}	$\frac{Q-Q_{BASE}}{\sqrt{3}V_{LL}} \frac{(1+\gamma_I)}{K_0}$	$\frac{Q-Q_{BASE}}{\sqrt{3}V_{LL}}(1+\gamma_I)$	$\frac{Q-Q_{BASE}}{\sqrt{3}V_{LL}} \frac{(1+\gamma_I)}{K_0}$	A_{RMS}

The two thyristors, or triac, that comprise the fail-normal switch on each phase of the D-CAP can be rated one of two ways. The voltages are the same as the equivalent AC switch voltages given by Table 10.1 for the three configuration, or $V_{THY} = V_{SW}$. However, the current depends on whether the thyristors are paired with a mechanical switch in high current and high power applications. If the thyristors are not paired with one, then they must be able to carry current continuously for an indefinite amount of time. This current is equal to the reactive current drawn by the main capacitor if it is connected directly to the grid. The RMS current is given by,

$$I_{THY} = \frac{\sqrt{2}}{\pi} V_S \omega C. \tag{10.11}$$

The factor, $\sqrt{2}/\pi$, is due to the fact that only a half-wave rectified current is going through each thyristor.

In high power or current applications, to reduce the high system cost from using large thyristors, mechanical switches such as circuit breakers may be paralleled to carry the continuous duty current while the thyristors provide quick response to faults. In such a scenario, the thyristors are rated for surge current, where most pulse-power thyristors can sink up to 20 times their nominal current rating for up to half a line cycle. As larger circuit breakers may not be able to respond within half a cycle, the rating ultimately depends on the response speed of the mechanical switches; the faster they are, the lower the thermal burden on the thyristors and lower their current rating.

10.3 Design of the AC Snubbers

The three AC snubber implementations are shown in Figures 10.4 and 10.5 integrated around an AC switch. Design equations to select the size and rating of the various components in the three implementations are presented in this section.

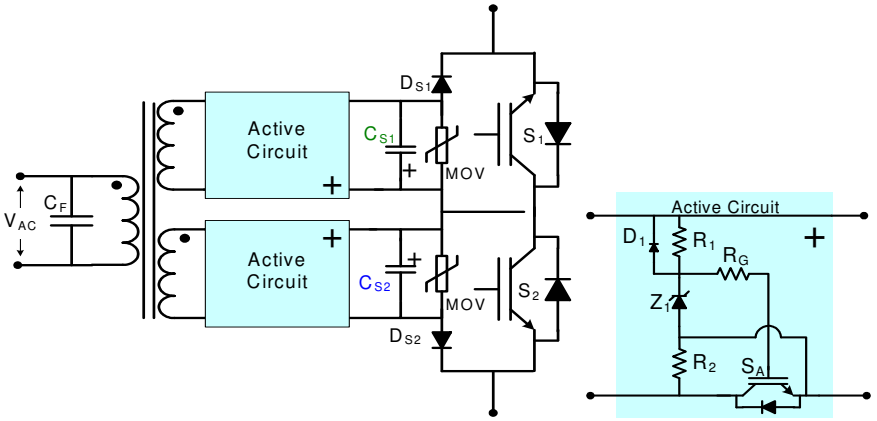


Figure 10.4: The AC snubber implemented using a low-frequency transformer and half-wave rectifying circuit.

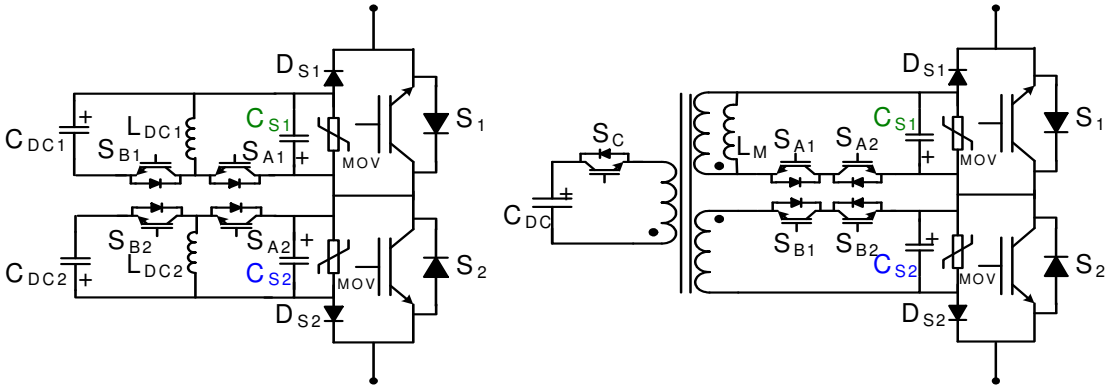


Figure 10.5: The AC snubber implemented using DC-DC converters with wide input range.

The snubber capacitors, C_{Sx}, for all three implementations of the AC snubbers are the same. They are sized based on the fundamental capacitor equation, $Cdv/dt = i$,

and are selected as follows:

$$C_{Sx} = I_{thresh}\frac{\Delta t}{\Delta v^*}, \tag{10.12}$$

where

$$\begin{aligned} I_{thresh} &\equiv \text{max current at which polarity error occurs,} \\ \Delta t = \frac{2}{f_C} &\equiv \text{the period of snubber operation,} \\ f_C &\equiv \text{the multi-step commutation frequency,} \\ \Delta v^* &\equiv \text{max allowable voltage surge due to snubber operation.} \end{aligned}$$

The snubber capacitors are sized based on the current that flows through it when the wrong commutation sequence occurs. The wrong commutation typically occurs when the current polarity cannot be sensed accurately enough, particularly around the zero crossings. In the four-step commutation [88], wrong current polarity can interrupt the current path for up to two steps. Thus, the max period over which the current is forced to flow through the snubbers is two times the commutation step period, or $\frac{2}{f_C}$.

The peak voltage of the snubber capacitors are the same as the switch rating plus a small DC or AC offset to reverse bias the snubber diodes:

$$V_{CS} = V_{SW} + V_{OFF}. \tag{10.13}$$

Fast recovery diodes are selected for the snubber diodes, D_{Sx}, that direct the energy to the snubber capacitors from the main power stage. The peak voltage across them are the same as the snubber capacitors, or,

$$V_{DS} = V_{SW} + V_{OFF}, \tag{10.14}$$

and peak surge current equal to the peak of the load current. The current rating seems high but this is a surge forward current, I_{FSM}, encountered during fault conditions.

Therefore, nominal diode rating can be 10 to 20 times lower, depending on the type of diode and/or the manufacturer,

$$I_{DS} = \frac{I_{SW}}{10}. \tag{10.15}$$

The MOVs are typically rated to breakdown at a voltage between the peak nominal of the snubber capacitor and the maximum voltage rating of the switches and devices.

10.3.1 Implementation 1

The IGBT switch, S_A, is rated to block the "negative" voltage in the secondary of the transformer, where the negative voltage is defined as the one that reverse-biases the anti-parallel diode of the switch. The voltage blocked by the switch is equal to the peak voltage of the snubber capacitor,

$$V_{SA} = V_{CS}. \tag{10.16}$$

The RMS current carried by the switch is equal to the reactive current of the snubber capacitor, approximated by,

$$I_{SA} = \omega C_S \frac{V_{CS}}{\sqrt{2}}, \tag{10.17}$$

where ω is the line frequency in rad/s and V_{CS} is the peak of the snubber capacitor voltage. The current rating of this implementation is extremely small and depends directly upon the value of the snubber capacitor.

The zener, Z_1, is selected to provide the reference voltage to turn the IGBT on, while the zener's forward drop provides the voltage to turn off the IGBT. Z_1 with $V_{Z1} = 15$ V reference is suitable for driving most IGBTs. Depending on the size of the snubber IGBT, the amount of gate charge, and how fast that gate charge has to be delivered, the zeners' power rating are selected accordingly. As the IGBT does not have to turn on during the first half of the positive half-wave, during which period the anti-parallel diode is charging the snubber capacitor, it does not have to be driven

very fast. Zeners with power ratings of 1-2 W are sufficient for driving most 1200 V IGBTs with less than 100 A rating. The resistor, R_1, biases the zener diode to develop its rated reference voltages while the resistor, R_2, limits the zener current when it is forward biased.

With a positive transformer secondary voltage, the zener, Z_1, imposes a positive gate-to-emitter voltage. Subsequently, the resistors, R_1 and R_G, drive charge into the IGBT and start to turn it on. During this period, the anti-parallel diode of the switch is forward biased and builds up the snubber capacitor voltage from zero to its peak. By a quarter of the line cycle later, the IGBT is fully activated to discharge the snubber capacitor back down to zero.

When a negative voltage appears on the transformer secondary, a negative DC reference voltage is developed by the forward drop of the zener, which turns off the IGBT. The diode, D_1, and gate resistor, R_G, carry charge out of the IGBT gate to enable the turn-off. Further, as soon as Z_1 and D_1 are forward biased, the snubber capacitor is negatively clamped to the sum of their forward voltage drops.

The resistor, R_1, is selected large enough to ensure that the zener's current does not exceed the maximum threshold, I_{ZM}, given by the zener's datasheet, and selected small enough such that there is adequate biasing current, I_{ZK}, at the minimum snubber voltage, $V_{CS|TH}$, to keep the snubber IGBT on. Therefore, R_1 is selected as follows:

$$R_{1|min} \leq R_1 \leq R_{1|max}, \tag{10.18}$$

where

$$R_{1|min} = \frac{V_{CS} - V_{Z1}}{I_{ZM}}, \tag{10.19}$$

$$R_{1|max} = \frac{V_{CS|TH} - V_{Z1}}{I_{ZK}}. \tag{10.20}$$

The resistor, R_2, limits the power dissipation on the zener when it is forward biased

and is selected based on,

$$R_2 \geq \frac{V_{CS}}{P_Z} V_{FZ}, \tag{10.21}$$

where

$$P_Z \equiv \text{power rating of the zener}, \tag{10.22}$$

$$V_{FZ} \equiv \text{forward voltage drop of the zener}. \tag{10.23}$$

The power rating of R_1 is given by,

$$P_{R1} = \frac{(V_{CS} - V_{Z1})^2}{\pi^2 R_1}, \tag{10.24}$$

and the rating for the resistor, R_2, is,

$$P_{R2} = \frac{(V_{CS})^2}{\pi^2 R_2}. \tag{10.25}$$

The gate resistor, R_G, is selected to be small as possible and still provide adequate damping of the parasitics, as calculated by,

$$R_{G|min} \geq 2\sqrt{\frac{L_{wire}}{C_{ies}}}, \tag{10.26}$$

where

$$L_{wire} \equiv \text{estimated module inductance},$$

$$C_{ies} \equiv \text{gate capacitance}.$$

Power rating of R_G is calculated as follows based on a triangular charge and discharge profiles:

$$P_G = 2I_{G|RMS}^2 R_G, \tag{10.27}$$

where

$$
\begin{aligned}
I_{G|RMS} &= I_{G|PK}\sqrt{\frac{k}{3}}, \\
I_{G|PK} &= \frac{V_{Z1} + V_{FZ}}{R_G}, \\
k &= \frac{t_p}{T_{grid}}, \\
t_p &\equiv \text{time width of the triangle pulse}, \\
T_{grid} &= \text{grid period}.
\end{aligned}
$$

This is a very conservative estimate of the power rating as the turn-on peak current is typically much lower due to the rate of charge transfer limited by R_1.

The voltage blocked by the diode D_1 depends on the maximum voltage drop across the resistor R_1, which is given by,

$$V_{D1} = V_{CS} - V_{Z1}. \tag{10.28}$$

The nominal RMS current is approximated by,

$$I_{D1} = I_{G|RMS} + \frac{V_{CS}}{\pi R_2}, \tag{10.29}$$

where $I_{G|RMS}$ is the RMS current during turn off of the IGBT and the second term is the RMS current averaged over a line cycle for the half-wave current that flows during the negative half-cycle of the transformer voltage.

The low-frequency transformer is rated based on the nominal VAR current drawn by the snubber capacitors plus any additional loading from gate-drive power supply. Due to the half-wave rectification, each transformer must be connected to two snubbers at minimum (positive and negative half-wave), or even number of snubbers when connecting to more than two. The total VA rating of the low frequency transformer to supply to two or more AC snubber circuits is calculated as:

$$S_{XFMR} = \frac{N}{2}\frac{V_{CS}^2}{2X_C}, \tag{10.30}$$

where

$$N \equiv \text{the total number of snubbers supplied,}$$

$$X_C \equiv \text{reactance of the snubber capacitor at the line frequency.}$$

With this implementation of the AC snubber, the low-frequency transformer can also be used to provide the energy for powering and operating the gate-drive circuitry to drive the main IGBT devices. The transformer ratings are increased accordingly.

10.3.2 Implementation 2: The Buck-Boost

The DC capacitor is sized based on the delta energy stored in a DC capacitor when its voltage is raised from V_{DC} to $V_{DC} + \Delta V_{DC}$,

$$\Delta E = \frac{1}{2} C_{DC} \left(\left(V_{DC} + \Delta V_{DC} \right)^2 - V_{DC}^2 \right). \tag{10.31}$$

Substituting for the delta energy, ΔE, that is being added to the capacitor and the desired voltage ripple, ΔV_{DC}, on the capacitor, the capacitor C_{DC} is solved for as follows:

$$C_{DC} = \frac{2 \left(E_{shuffle} + E_{GD} \right)}{2 \Delta V_{DC} V_{DC} + \left(\Delta V_{DC} \right)^2}, \tag{10.32}$$

where

$$E_{shuffle} = \frac{1}{2\eta} C_S \left(V_{CS}^2 - V_{OFF}^2 \right),$$

$$E_{GD} = \frac{3}{4} \int_t^{t+T_{grid}} P_{GD}(\tau)\, d\tau,$$

$$V_{DC} \equiv \text{minimum DC voltage of the DC capacitor,}$$

$$\Delta V_{DC} \equiv \text{peak-to-peak voltage ripple on the DC capacitor,}$$

$$V_{CS} \equiv \text{peak voltage on the snubber capacitor,}$$

$$V_{OFF} \equiv \text{DC offset on the snubber voltages,}$$

$$P_{GD}(t) \equiv \text{power drawn by the gate drive PCB,}$$

$$\eta \equiv \text{conversion efficiency.}$$

$E_{shuffle}$ is the energy shuffled from the DC capacitor to the snubber capacitor when charging from its DC offset to the peak voltage during quarter of a line cycle. E_{GD} is the energy pulled from the line over quarter of a line cycle to compensate for the losses in the gate driver.

For a desired peak-to-peak current ripple of Δi_L, and assuming the converter is operating at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM), the inductor is sized using,

$$L_{DC} = \frac{1}{f_S} \frac{V_{DC|PK}}{\Delta i_L}, \tag{10.33}$$

where

$$V_{DC|PK} = V_{DC} + \Delta V_{DC},$$
$$f_S \equiv \text{switching frequency of the converter,}$$

Here, the largest duty cycle to charge up the snubber capacitor is assumed to be near unity when large amount of charge has to be transferred from a low-voltage DC capacitor to a snubber capacitor of relatively high voltage. This condition typically occurs when the snubber voltage first starts to get regulated.

The peak voltage and the RMS current of the two switches are given by,

$$V_{Sx} = V_{CS} + V_{DC|PK}, \tag{10.34}$$
$$I_{Sx} = \frac{\Delta i_L}{\sqrt{3}}. \tag{10.35}$$

10.3.3 Implementation 2: The Flyback

Assuming the flyback transformer has a $1:1:1$ turn ratios, the current and voltage ratings of the switches remain the same. The magnetizing inductance takes on the same value as the switching inductor of the buck-boost design as well. The peak

voltage and the RMS current rating of the transformer is then,

$$V_{XFR} = V_{CS}, \tag{10.36}$$

$$I_{XFR} = \frac{\Delta i_L}{\sqrt{3}}. \tag{10.37}$$

As the converter is operating in a DCM, the high-frequency transformer is not at the risk of saturating. However, care must be taken in the controller to ensure that the magnetizing current resets to zero at the end of every switching period.

The DC capacitor is sized using Equation 10.32, but with the energy, E_{GD}, given by,

$$E_{GD} = \frac{1}{4} \int_{t}^{t+T_{grid}} P_{GD}(\tau)\, d\tau. \tag{10.38}$$

Here, the energy is one-half lower than the case for the buck-boost because the DC capacitor is charged every half-cycle, as opposed to every other half-cycle, so less energy is drawn per charge.

10.4 Example Design 1: A Low-Voltage Application

A project calls for a D-CAP system operating at 480 V / 60 Hz to provide 200 kVAR worth of dynamic and 50 kVAR of base VAR compensation for an industrial facility. The three low-voltage D-CAP configurations are implemented exactly as depicted in Figure 10.1. The devices are operated at a switching frequency of 10 kHz. The design results are presented in Table 10.3, which summarizes the passive component values as well as the peak voltage and the RMS current of the various components and devices.

The voltage and current rating of the devices and components are based on the listed numbers plus the added overhead safety margins to account for transients, disturbances, and harmonic compensation. The final ratings depend on the availability of components and devices as well as designer's preferences in rating for safety margins. Due to these various factors, only the actual peak voltage and current in

Table 10.3: The design results of the primary power stage for a 250 kVAR D-CAP operating at 480 V / 60 Hz.

Components	Configurations			
	Buck	Boost	Buck-Boost	
Nominal Duty, $K_{0\|NOM}$	0.707	0.2	0.5	
Max Duty, $K_{0\|MAX}$	1	0.333	0.6	
C	4.61	1.47	2.3	(mF)
	390	490	390	(V)
C_{F1}	450	530	190	(μF)
	390	390	390	(V)
C_{F2} (10% ripple)	130	47	390	(μF)
	430	430	430	(V)
L_{F1}	22	60	7.2	(μH)
	250	250	280	(A)
L_{F2} (30% ripple)	96	44	31	(μH)
	440	310	630	(A)
AC switch	390	490	780	(V)
	440	310	630	(A)
Single Thyristor	490	780	790	(V)
	220	69	110	(A)

the converters are listed. As an example, for the range of voltage rating of the AC switches, 1200 V IGBT devices should be adequate. For the calculated current rating, 800 A devices for the boost, 1200 A devices for buck, and 1600 A devices for the buck-boost with roughly 50 percent overhead margins are selected. These devices are readily available off-the-shelf from companies such as Dynex Semiconductor™ and Infineon Technologies™.

The inductors are typically a custom product and need to be built with a suitable core material with relatively low losses and high permeability like powder iron. The filter capacitors are obtainable from vendors such as Electronic Concepts at various voltage and current ratings. The main capacitor is typically a PFC capacitor and can be purchased based on VAR requirements. If enough capacitance cannot be obtained

in a single package, multiple units are paralleled.

The buck-boost implementation of the AC snubber is selected in providing safe commutation and fault tolerance for the three converters. The following assumptions are made regarding the operation of the D-CAP and the snubbers:

- current-based commutation used,
- multi-step commutation frequency of $f_C = 800$ kHz,
- current sensors have 100 percent polarity confidence outside of a ± 5 A band,
- max voltage ripple allowed on the snubber capacitors per snubbing event is 5 percent of the peak nominal voltage,
- the DC capacitor has a constant 5 W loading from control supply,
- the DC-DC converter has an efficiency of 98 percent,
- the switching frequency of the DC-DC converter is 20 kHz.

Only a single AC snubber circuit per phase is required in this design example. The values and ratings of the various components are summarized by Table 10.4, rounded up to one or two significant digits. The final circuit diagrams of the three D-CAP systems are given by Figure 10.6. The snubber is equivalently represented with two diodes and a voltage source.

10.5 Example Design 2: A Medium-Voltage Application

The second design calls for a D-CAP configuration operating at 2.4 kV / 60 Hz to provide up to 1.8 MVAR under nominal grid conditions with base VAR requirement of 225 kVAR. IGBTs with 1200 V rating are series connected to scale the D-CAP to this voltage level as discussed in Section 9.5 and operated with the switching frequency of 10 kHz. Since the resulting topology is still basically the same two-level

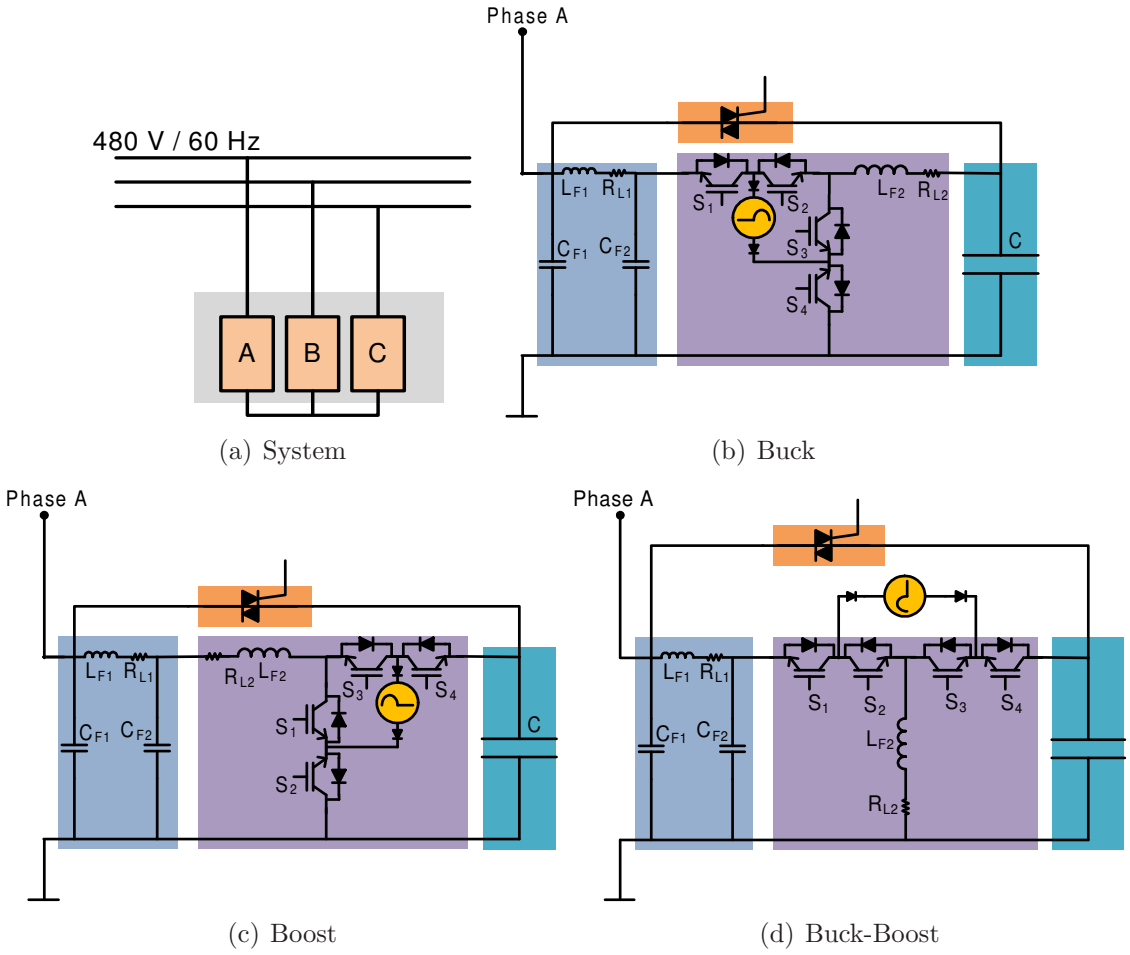
Table 10.4: The design results of the buck-boost AC snubber for a 250 kVAR D-CAP operating at 480 V / 60 Hz.

Components	Configurations			
	Buck	Boost	Buck-Boost	
C_S	0.63	0.51	0.32	(μF)
	400	500	790	(V)
C_{DC}	1.8	2.1	2.7	(mF)
	27	27	27	(V)
D_{S1} and D_{S2}	200	250	400	(V)
	63	45	89	(A_{PK})
L_{DC}	260	260	260	(μH)
	$5/\sqrt{3}$	$5/\sqrt{3}$	$5/\sqrt{3}$	(A)
S_A and S_B	430	530	820	(V)
	$5/\sqrt{3}$	$5/\sqrt{3}$	$5/\sqrt{3}$	(A)
MOV	600	700	1000	(V)

implementation, except for the series-connected devices, the design equations can be applied directly. Table 10.5 summarizes the component size, and peak voltage and RMS current for the three different configurations of the D-CAP.

For the calculated device ratings, six (three AC switches) 1200 V IGBTs of 1800 A capacity are connected in series for the buck, eight (four AC switches) 1200 V IGBTs of 1600 A capacity for the boost, and 10 (five AC switches) 1200 V IGBTs of 2400 A capacity for the buck-boost in order to realize one equivalent AC switch. Two equivalent AC switch per phase, and six per three-phase unit are required for implementation. This implies that the total number of IGBTs required for the three-phase operation is then 36, 48, and 60 for the buck, boost, and buck-boost, respectively. As the current levels are quite high, passive components will have to be paralleled to keep the parasitic losses low. An alternate implementation would be to parallel two units per phase such that the current ratings can be halved, requiring double the number of total devices at half the current rating.

When selecting the inductor, L_{F2}, care must be taken to ensure the characteristic



(a) System (b) Buck

(c) Boost (d) Buck-Boost

Figure 10.6: System and phase A sub-system schematics of the example design 1.

frequency, $\omega_0 = 1/\sqrt{L_{F2}C}$ does not coincide at the same frequency as the harmonics generated by the load.

The low-frequency implementation of the AC snubber is selected in providing safe commutation, fault tolerance, and equal voltage sharing for the three converters. The following assumptions are made regarding the operation of the D-CAP and the snubbers:

- current-based commutation used,
- multi-step commutation frequency of $f_C = 800$ kHz,
- current sensors have 100 percent polarity confidence outside of a ± 5 A band,

Table 10.5: The design results of the primary power stage for a 1.8 MVAR D-CAP operating at 2.4 kV / 60 Hz.

Components	Configurations			
	Buck	Boost	Buck-Boost	
Nominal Duty, $K_{0\|NOM}$	0.707	0.2	0.5	
Max Duty, $K_{0\|MAX}$	1	0.333	0.6	
C	1.45	464	725	(μF)
	2	2.4	2	(kV)
C_{F1}	63	88	50	(μF)
	2	2	2	(kV)
C_{F2} (10% ripple)	41	15	123	(μF)
	2.2	2.2	2.2	(kV)
L_{F2} (30% ripple)	300	140	98	(μH)
	700	490	990	(A)
L_{F1}	70	190	23	(μH)
	400	390	410	(A)
AC Switch	2	2.4	3.9	(kV)
	700	490	990	(A)
Single Thyristor	2	2.4	3.9	(kV)
	340	110	170	(A)

- max voltage ripple allowed on the snubber capacitors per snubbing event is 5 percent of the peak nominal voltage.

An AC snubber is integrated around each IGBT in this design example. A single low-frequency transformer with multiple secondary windings is used per phase to supply an AC voltage to the snubber circuits. The component values and peak voltage and RMS current of the various components and devices are summarized by Table 10.6, rounded to two significant digits. The final circuit diagrams of the three D-CAP systems are given by Figure 10.7. The snubber is equivalently represented with a diode and a voltage source for simplicity. The final voltage and current ratings are based on the tabulated values plus some overhead safety margins.

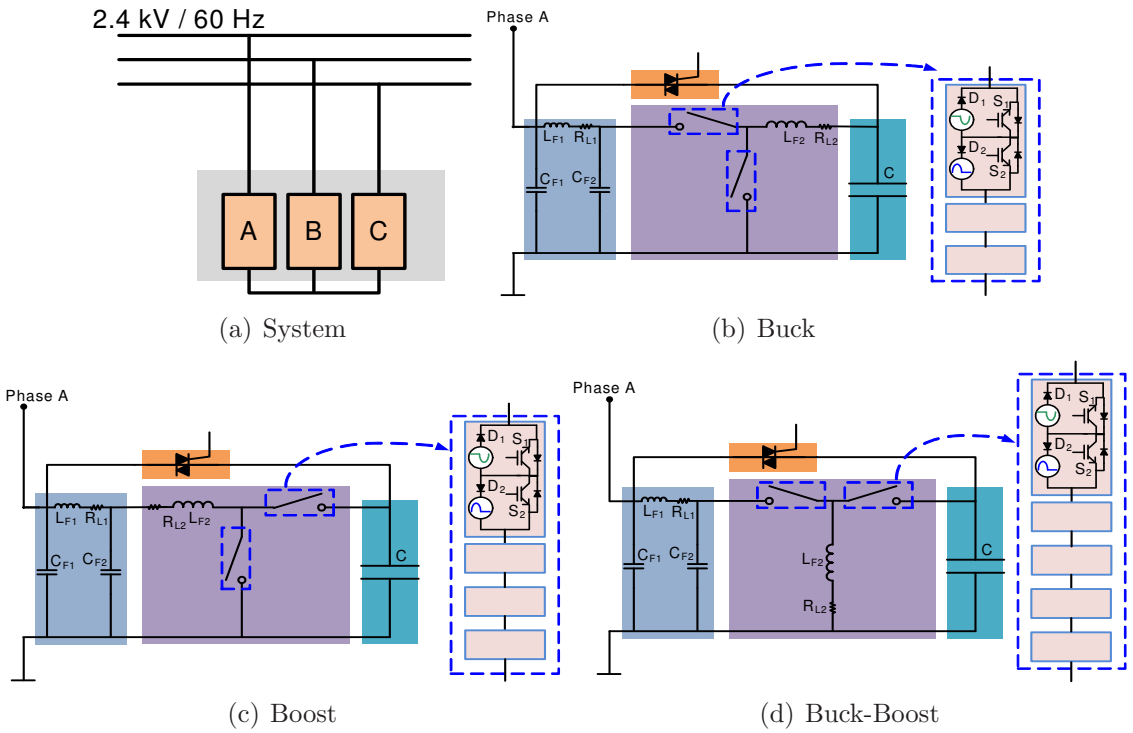
Table 10.6: The design results of the low-frequency AC snubber for a 1.8 MVAR D-CAP operating at 2.4 kV / 60 Hz.

Components	Configurations			
	Buck	Boost	Buck-Boost	
Total number of snubbers	12	16	20	
C_S	0.38 660	0.41 620	0.32 790	(μF) (V)
D_1	640 120	600 100	770 140	(V) (mA)
D_S	660 99	620 70.0	790 140	(V) (A_{PK})
R_1	20 2	20 2	20 3	(kΩ) (W)
R_2	10 4	10 4	10 6	(kΩ) (W)
R_G	0.5 << 0.5	0.6 << 0.5	0.5 << 0.5	(Ω) (W)
S_A	650 70	620 70	790 70	(V) (mA)
MOV	800	800	1000	(V)
Transformer per phase	190	230	370	(VA)

10.6 Example Design 3: A Medium-Voltage Application

The third design calls for a D-CAP configuration operating at 13.8 kV / 60 Hz to provide up to 10 MVAR under nominal grid conditions with base VAR requirement of 1 MVAR. In this example, the D-CAP is scaled up using the cascaded cells approach outlined in Section 9.7. IGBT devices with 1.2 kV ratings are selected for scaling, with the switching frequency of 10 kHz; this is assuming adequate thermal management is in place. With devices of this rating, five cells per phase are selected to scale to 13.8 kV. The topology is designed modularly where each cell injects equal fraction of the total VARs. The design is presented in Table 10.7 for a single cell.

For the calculated device ratings, six (three AC switches) 1200 V IGBTs of 1800



(a) System (b) Buck

(c) Boost (d) Buck-Boost

Figure 10.7: System and phase A sub-system schematics of the example design 2.

A capacity for the buck, eight (four AC switches) 1200 V IGBTs of 1600 A capacity for the boost, and 12 (six AC switches) 1200 V IGBTs of 2400 A capacity for the buck-boost are connected in series in order to realize one equivalent AC switch. Two equivalent AC switch per cell, and 15 cells per three-phase unit are required for the implementations. This implies that the total number of IGBTs required for the three-phase operation is 180, 240, and 360 for the buck, boost, and buck-boost, respectively. As the current levels are quite high, passive components will have to be paralleled to keep the parasitic losses low. An alternate implementation would be to parallel two units per phase such that the current ratings can be halved, requiring double the number of total devices at half the current rating.

In the design of the buck-boost D-CAP, as the capacitor, C_{F2}, is sized large enough to meet the base VAR requirements, the capacitor, C_{F1}, is sized with the minimum value of 10 μF.

Table 10.7: The design results of the primary power stage for a single cell for a 10 MVAR D-CAP operating at 13.8 kV / 60 Hz.

Components	Configurations			
	Buck	Boost	Buck-Boost	
IGBTs per cell	6	8	12	
Nominal Duty, $K_{0\|NOM}$	0.707	0.2	0.5	
Max Duty, $K_{0\|MAX}$	1	0.333	0.6	
C	1.25	0.401	0.627	(mF)
	2.3	2.8	2.3	(kV)
C_{F1}	35	57	10	(μF)
	2.3	2.3	2.3	(kV)
C_{F2} (10% ripple)	35	13	110	(μF)
	2.5	2.5	2.5	(kV)
L_{F1}	80	220	26	(μH)
	400	380	410	(A)
L_{F2} (30% ripple)	350	160	110	(μH)
	690	490	980	(A)
AC Switch	2.3	2.8	4.5	(kV)
	690	490	980	(A)
Thyristors	2.3	2.8	4.5	(kV)
	340	110	170	(A)

The total number of IGBTs required for the buck-boost topology is roughly 85 percent of the sum total of the buck and boost combined together. This is expected, as theoretically the buck-boost is able to provide both the buck and boost functionality. Thus, one can either parallel the buck and boost together, or use a single buck-boost unit to provide the same functionality. However, the high current rating of the buck-boost going through almost twice the number of IGBTs can induce significant amount of losses. Furthermore, the filter requirements are also greater in the buck-boost for the same level of THD.

The flyback implementation of the AC snubber is selected in providing safe commutation, fault tolerance, and voltage sharing for the three converters. The following

assumptions are made regarding the operation of the D-CAP and the snubbers:

- current-based commutation used,
- multi-step commutation frequency of $f_C = 800$ kHz,
- current sensors have 100 percent polarity confidence outside of a ± 5 A band,
- max voltage ripple allowed on the snubber capacitors per snubbing event is 5 percent of the peak nominal voltage,
- the DC capacitor has a constant 10 W loading from control supply,
- the DC-DC converter has an efficiency of 98 percent,
- the switching frequency of the DC-DC converter is 20 kHz.

One dual-output flyback snubber per AC switch is required in this design example. The values and ratings of the various components are summarized by Table 10.4, rounded to two significant digits. The final circuit diagrams of the three D-CAP systems are given by Figure 10.8. The flyback snubbers are equivalently represented with two diodes and two voltage sources per snubber.

10.7 Design Validation with Simulation

Designs of the three configurations in the second example are simulated with their respective switching models. The results are given by Figure 10.9. The synchronous-reference-frame control architecture discussed in Chapter 7 is employed in generating the results. All three topologies are very effective in suppressing the harmonics, and ensuring that adequate voltage support is in place.

The VAR injection is demonstrated in the form of power factor correction, as observable in Figure 10.9(a). In comparing the three topologies in Figure 10.9(b), the boost is able to provide the same level of harmonic compensation with the lowest

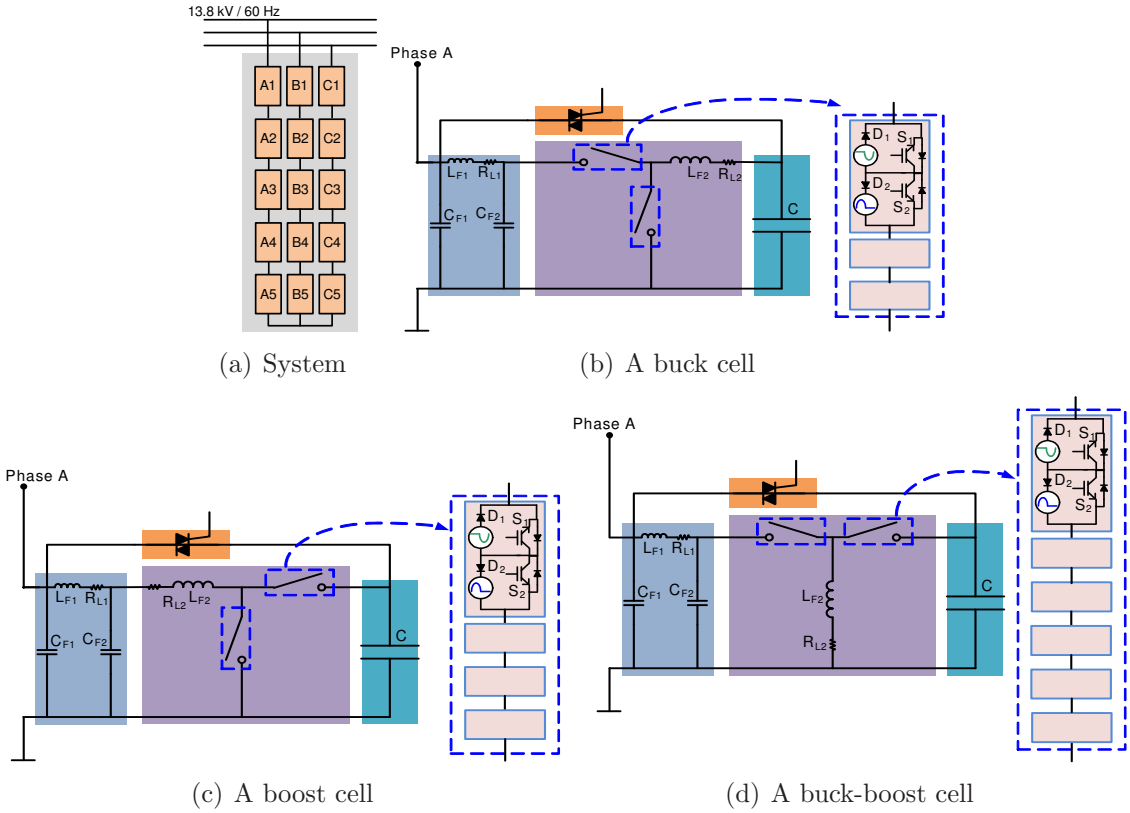
Table 10.8: The design results of a single flyback AC snubber for a 10 MVAR D-CAP operating at 13.8 kV / 60 Hz.

Components	Configurations			
	Buck	Boost	Buck-Boost	
C_{DC}	2.3 27	2.2 27	2.3 27	(mF) (V)
C_{Sx}	0.33 760	0.35 710	0.33 760	(μF) (V)
D_{Sx}	760 98	710 70	760 140	(V) (A_{PK})
L_M	260 $5/\sqrt{3}$	260 $5/\sqrt{3}$	260 $5/\sqrt{3}$	(μH) (A)
Switches	790 $5/\sqrt{3}$	740 V $5/\sqrt{3}$	780 $5/\sqrt{3}$	(V) (A)
MOV	1000	900	1000	(V)

peak-to-peak duty excursions. The boost also has the same or lower current rating than the buck. However, the downside is that the voltage stresses are higher with the boost. The buck-boost is the only topology that comes close to spanning the operating domain of an ideal VAR compensator but has the highest current and voltage stresses, and highest duty excursions. Thus, buck-boost designs tend to be costly. An alternative to the buck-boost configuration is to instead parallel buck and boost together with devices that are roughly half the rating.

10.8 Conclusions

Equations to determine size and ratings of the devices and various passive components in the primary power stage as well as the AC snubbers are presented in this chapter. Based on these equations, three different design examples are discussed. These designs validate that the D-CAP topologies are scalable from low to medium voltages with widely available devices and components. The operation and performance of the second design are validated through simulation results and all three configurations of



(a) System (b) A buck cell

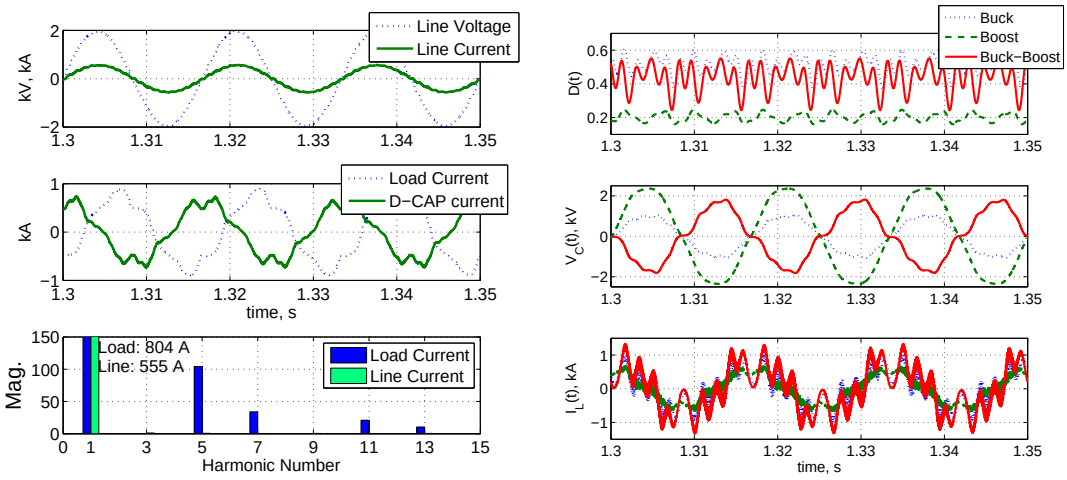
(c) A boost cell (d) A buck-boost cell

Figure 10.8: System and phase A sub-system schematics of the example design 3.

the D-CAP were found to be effective in meeting the design objectives.

In all three example designs, one obvious difference between the buck and boost configurations is that the boost topology is able to provide the same level of compensation with lower capacitance, whereas the buck-boost is somewhere in-between. Due to high dV/dt stresses on the buck-boost topology, the component and device ratings are overall much higher.

All three topologies are able to dynamically vary their supply of reactive power, as needed by the system and/or load whose load profiles are in constant flux throughout the day. But dynamic compensation comes at the cost of semiconductor devices. By relegating the static supply of reactive power to passive components, the switches can be rated to provide only the dynamic VAR requirement of the system, thereby reducing the cost of the overall DVHC system. The presence of the filter capacitors,



(a) (b)

Figure 10.9: Simulation results depicting **a**) line voltage/current (top), load current and D-CAP current (middle), and FFT of line and load current (bottom) for all three configurations of D-CAP, and **b**) the duty function (top), the voltages across the main capacitors C (middle), and the current through the filter inductor, I_{LF2}, for the buck, the boost, and the buck-boost configurations of the D-CAP.

C_{F1} and C_{F2}, in the D-CAP provide the dual functionality of suppressing switching harmonics and meeting the base VAR requirements of the system. However, in certain designs, large capacitors for suppressing switching harmonics may result in excess static supply of reactive power. To address this, the designer can go through an iterative process to either tweak the value of the main capacitor, C, or lower the THD specifications of the converter. The former approach results in reduced dynamic range, while the latter degrades spectral performance of the converter. These limitations are especially true for a buck-boost design, which may restrict its applications.

Boost D-CAP has the potential for the best performance at a lower cost, especially for operating in conditions where the grid voltages are sub-nominal. However, for the widest operating range and leveraging the need to lower current ratings of the various components, the buck and boost topologies can be operated in parallel.

CHAPTER XI

EXPERIMENTAL VALIDATION

11.1 Introduction

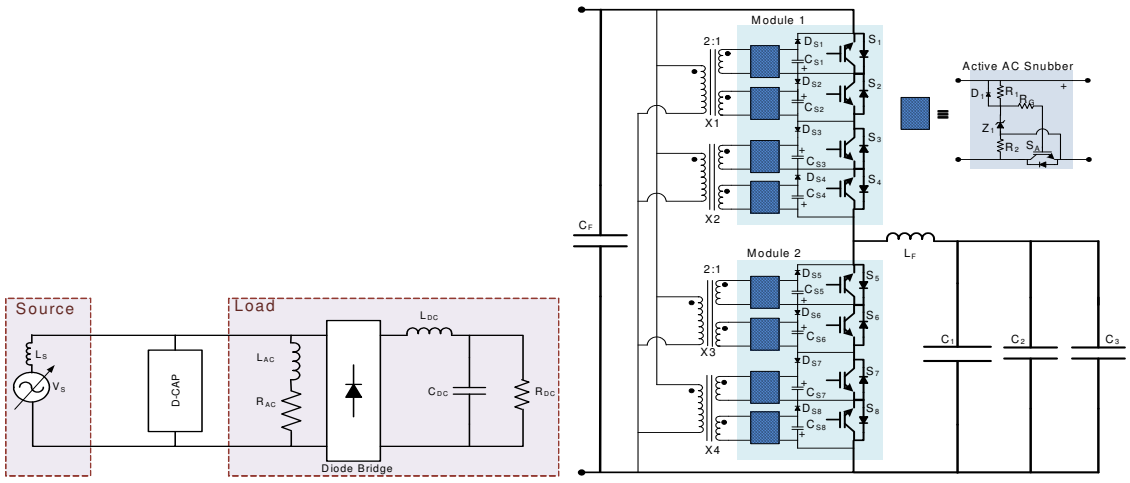
In validating the operation of the D-CAP and the underlying concepts, a single-phase medium-voltage prototype capable of providing up to 40 kVAR of VAR and harmonic compensation is designed, fabricated and tested.

11.2 System Schematic

A proof-of-concept prototype of the buck D-CAP is built with series-connected devices, where four IGBTs are used on the top arm and four on the bottom. The low-frequency implementation of the AC snubber is used, where a snubber is integrated around each device. The D-CAP compensates for a harmonic-rich load comprised of a diode-rectifier in parallel with a series-connected resistor and inductor.

The system and the D-CAP schematics are depicted by Figure 11.1(a) and Figure 11.1(b), respectively. The primary capacitance in the D-CAP is obtained by paralleling three capacitors, C_1-C_3. A single capacitor, C_F, is used on the input side as a filter. The filter capacitor and source inductance are adequate in providing second order filtering and preventing unwanted switching harmonics from propagating into the grid.

For implementing the active AC snubber, four low-frequency transformers are used; one per AC switch. Although one transformer would typically be used per module, the unavailability of off-the-shelf transformers with appropriate ratings and four output windings mandated the approach depicted in Figure 11.1(b).



(a) System (b) D-CAP

Figure 11.1: The system and the D-CAP schematic.

The selection of the components in the D-CAP prototype, including the components used in the AC snubber, are summarized by Table 11.1.

11.3 Control and Hardware Architecture

The D-CAP is built as a modular AC power electronics building block (AC PEBB), where each module is comprised of two AC switches with associated snubber and auxiliary components, as shown in Figure 11.1(b). The conceptual mechanical layout of the D-CAP is depicted in Figure 11.2(a), which is organized as two modules with a three-layer stack each. One module forms the top arm, while the second module forms the bottom arm of the D-CAP.

The bottom layer of each module is the power stage comprised of four IGBT devices in the TO-247 package mounted onto a heat sink. A printed circuit board (PCB) interfaces the devices and establishes electrical connection for conducting up to 50 A of peak current. The snubber diodes, snubber capacitors, snubber switches, and circuit for driving the snubber switches are all on this PCB.

The second layer interfaces the controller with the power stage and consists of a

Table 11.1: The component values used for the experimental prototype of the buck D-CAP.

Component	Value		Description
L_{AC}	1.2	mH	AC load inductor
R_{AC}	8	Ω	AC load resistor
L_{DC}	25	mH	DC load inductor
C_{DC}	1.5	mF	DC load filter capacitor
R_{DC}	20	Ω	DC load resistor
C_1	153	μF	Main capacitor 1
C_2	100	μF	Main capacitor 2
C_3	100	μF	Main capacitor 3
C_F	100	μF	Input filter capacitor
L_F	200	μH	Switching inductor
S_1-S_8	1200	V	Voltage rating of the main IGBT + diode
	100	A	Current rating of the main IGBT + diode
D_1-D_8	1200	V	Voltage rating of snubber diodes
	20	A	Current rating of snubber diodes
Switch, S_A	1200	V	Voltage rating of snubber IGBT
	3	A	Current rating of snubber IGBT
D_1	600	V	Voltage rating of driving diode
	2	A	Current rating of driving diode
C_{S1}-C_{S8}	0.16	μF	Snubber capacitors
R_1	200	kΩ	Snubber circuit resistor 1
R_2	400	kΩ	Snubber circuit resistor 2
R_g	4.7	Ω	Drive resistor for snubber IGBT
Z_1	15	V	Voltage rating of snubber zener
Transformer	150	VA	Power rating of the low-frequency transformer
MOV	1000	V	Voltage rating of the MOV

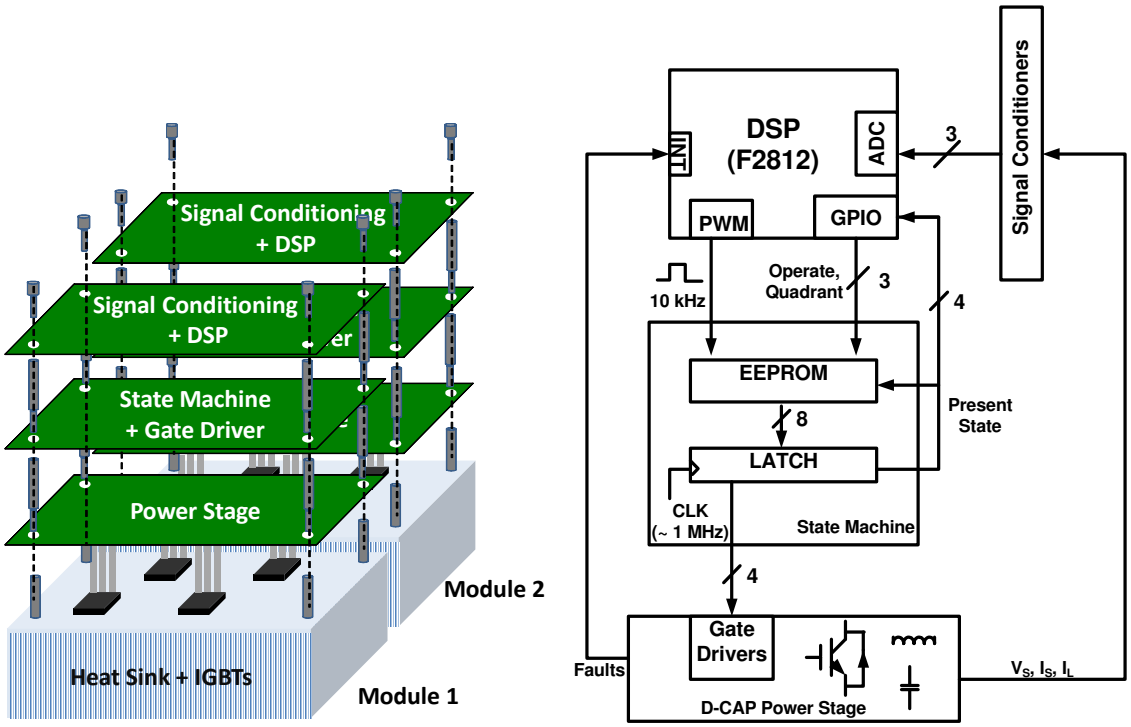
PCB that houses the state machine for providing four-step current-based commutation, and gate drivers that take the logic outputs of the EEPROM and synthesize the power signals for commutating the four IGBTs. The finite state machine is implemented using an 8-bit EEPROM with a clocked latch.

The third layer houses the primary controller and is comprised of a PCB that provides signal conditioning and an interface to a DSP board. The current and

voltage information required by the controller must be filtered of noise, and scaled-down and level-shifted to be within 0 to 3 V band. These three functionalities are provided by the signal-conditioning circuits. The analog-to-digital converter (ADC) built within the DSP is used to convert the analog signals to digital. The DSP acts upon these signals to provide ideal duty cycles and operating mode information to the state machine in the second layer.

The dimension of the bottom PCB is 9.35 by 4.45 inches, while the dimensions of the top two PCBs are 9.35 by 4.20 inches. Threaded standoffs are utilized to provide adequate spacing and mechanical rigidity between each PCB.

The filter inductor, filter capacitors, and main capacitors are located external to the modules and are connected to the PCBs through terminal housings.



(a) Mechanical architecture (b) Control architecture

Figure 11.2: Mechanical and control hardware architectures in fabricating the modular buck D-CAP.

The sketch of the control architecture is depicted in Figure 11.2(b). The grid

voltage, V_S, grid current, I_S, and inductor current, I_L, are measured. The grid voltage is used as an input to the software-based phased locked loop (PLL) within the DSP, which is necessary for even harmonic modulation when providing harmonic filtering. The source current is used as a feedback to drive the harmonic components to zero and to maintain unity power factor at the PCC. The inductor current is used to assess polarity for determining the correct commutation sequence. These three measurements are fed through the signal-conditioning circuits before going through the DSP's ADC.

Various fault signals are OR'ed together and the output signal is fed to the DSP as an external interrupt to execute a fault-response algorithm.

The DSP (controller) generates an ideal PWM signal, quadrant information for reflecting current polarity, and operate logic for toggling standby mode under fault contingencies. These three signals, along with state-feedback from the latch, form the input to the EEPROM, which is programmed with a finite-state machine. The eight-bit output of the EEPROM are latched with a high-frequency clock that determines the speed of the four-step commutation. The four most significant bits of the latch output are the input to the gate drivers, while the least four significant bits are the state numbers that are used as the four least significant address bits of the EEPROM.

11.4 Power Stage

The entire D-CAP prototype is mounted onto one large heat sink, as opposed to assigning one heat sink for every module. The heat sink is Wakefield Engineering's extruded high fin density of model 510-12M with a base plate dimension of 7.38 by 12 inches and with a thermal resistance under natural convection of 0.24 °C/W.

International Rectifier's IRGPS60B120KDP 1200 V, 105 A IGBT with integrated anti-parallel diode on a TO-247 package is selected for the main devices. The devices

are mounted onto the heat sink with an electrically insulating but thermally conducting material. These thermal pads are necessary for insulating the IGBTs from each other and the heat sink. Bergquist's Q-Pad 3 with a thermal resistivity of 0.35 °C/W is selected.

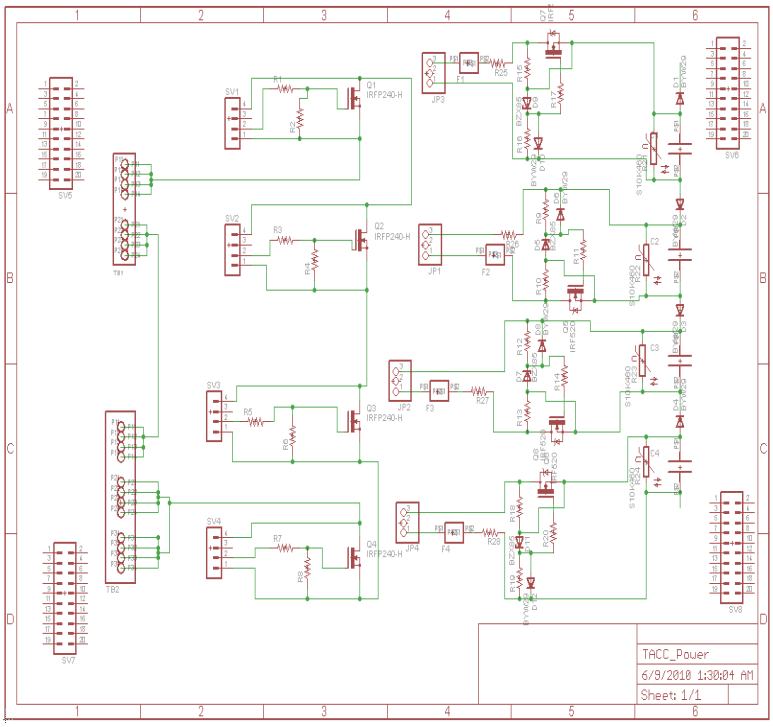
The schematic and CAD drawing of the PCB that forms the power stage of the two modules for inter-connecting the IGBTs and various passive components and snubber circuits are shown in Figure 11.3. With a dimension of 9.35 by 4.45 inches, two identical boards are mounted side by side on the heat-sink along the heat-sink's long axis, such that about 2 inches of the two PCBs extend above and below the heat sink. Snubber transformers, gate drivers, filter capacitors and inductors, and main capacitors are installed externally and connected to the power stage PCB through terminal pins and clamps designated by JP1-JP4, SV1-SV4, and TB1-TB2.

The inductor, L_F, is built around the Micrometals T400-14D iron powder core with 75 turns of a litz wire. The magnetic core properties are summarized by Table 11.2.

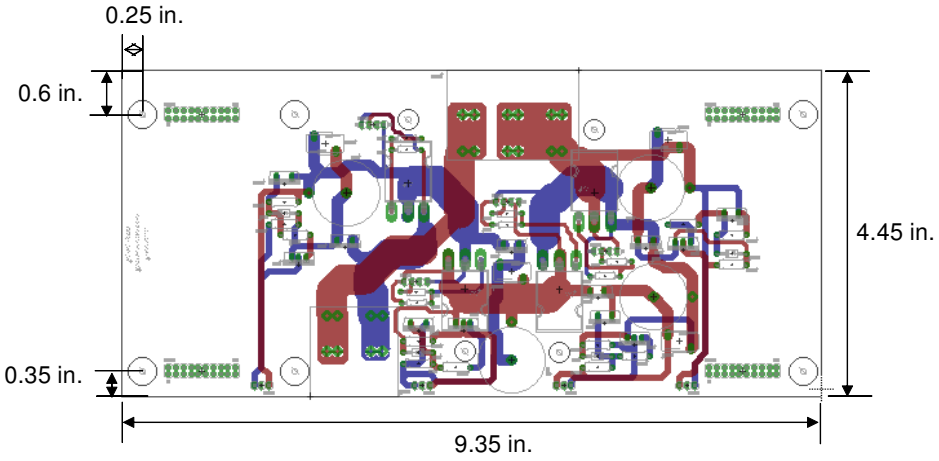
Table 11.2: Properties of the selected Micrometals T400-14D core.

Parameters	Value		Description
OD	102	mm	Outer dimension
ID	57.2	mm	Inner dimension
Ht	33	mm	Height
l	25	cm	Flux path length
A	6.85	cm^2	Cross-sectional area of flux path
μ_0	14	$H{\cdot}m^{-1}$	Reference relative permeability

Metallized polypropylene capacitors manufactured by Electronic Concepts under the part number 5MPA2107J are selected for the three 100 μF capacitors, C_2, C_3, and C_F. Aerovox AMP0025F33S with 153 μF capacitance is used as one of the main capacitors, C_1.



(a) Schematic

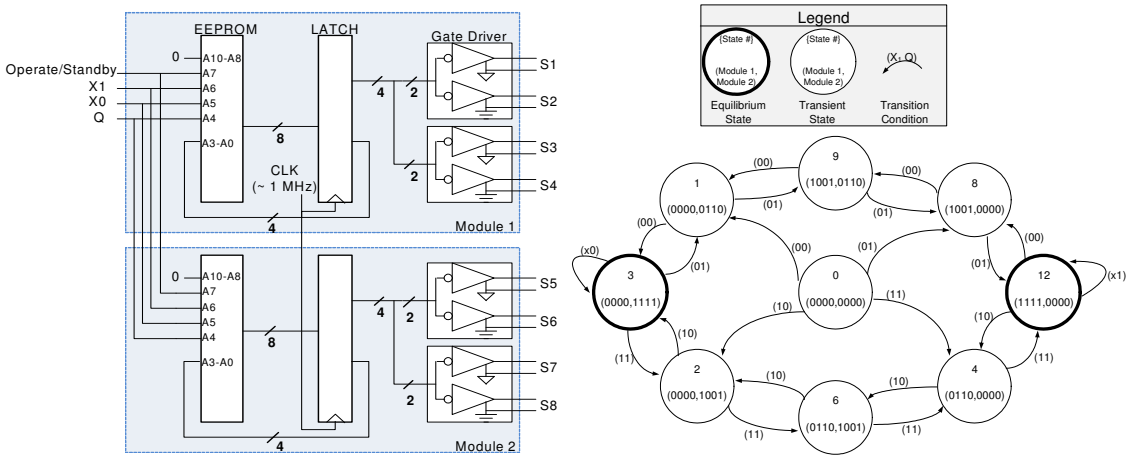


(b) PCB

Figure 11.3: Schematic and CAD design of the power stage PCB.

11.5 State Machine and Gate Drivers

The second or middle PCB houses the gate drivers and the state machine for driving the devices based on an ideal duty signal and inductor current polarity. The state machine implements the four-step current-based commutation, which is necessary for safely commutating the AC switches. Figure 11.4(a) demonstrates how based on the logic signals from the controller PCB, the gate drive PCB generates the necessary power signal for controlling the IGBTs.



(a) Hardware implementation (b) State diagram

Figure 11.4: Implementation of the finite state machine.

The state machine is implemented with an ON Semiconductor CAT28C16ALI90 8-bit EEPROM and a Texas Instruments SN74ALS996NT 8-bit latch. The high frequency clock for the latch is synthesized using a 555-type oscillator circuit designed around the Intersil's ICM7555 chip. The finite state machine diagram with non-inverted output signals for driving the gate drivers are given by Figure 11.4(b). Each circle indicates a state number on the top and two sets of four-bit binary numbers on the bottom. The first set of four bits are the non-inverted logic signals to control the four IGBTs on the top arm and the second set of four bits are used to control the IGBTs on the bottom arm. State transition occurs when either the current polarity

bit, X_1, or the PWM signal, Q, changes. When the inductor current has a positive value when flowing into the main capacitors, the X_1 bit is high. The voltage polarity bit, X_0, is not implemented in the state machine as the voltage-based commutation is not employed in the prototype. Only the nominal operating states are depicted in the figure. The gate drivers take inverted logic inputs, therefore the output bits in the finite state machine diagram are all inverted when programming the EEPROMs.

Powerex BG2A gate driver board, which is a commercial gate driver built around VLA500-01 gate driver chips, is selected for controlling the IGBTs. Two BG2A boards, capable of driving two devices per board, are installed on each of the two PCBs. These gate drivers take an inverted logic input. Braided wires, which minimize interference and radiation, are used to connect the output of the gate drivers to the power stage. The PCB design is given by Figure 11.5, which shows the state machine located in the center of the board and flanked by the two BG2A boards.

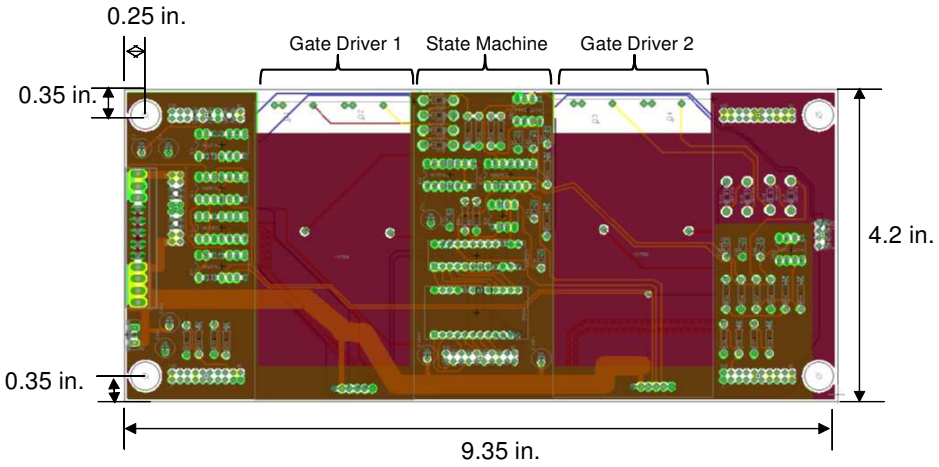


Figure 11.5: PCB design of the gate-drive stage.

11.6 Signal Conditioner and Controller

Voltage measurement of the grid is made through a hall-effect sensor manufactured by LEM under the model LV 100-750, while currents are sensed through Pearson 110A

probes. The outputs of both sensors are voltages that are sinusoidal, potentially larger than the allowable 0 to 3 V band of the ADC, and may contain some amount of high-frequency noise or spikes. To condition and prepare the sensed signals for the ADC, the circuit shown in Figure 11.6 is employed. The first stage scales the signal by a factor of $A_1 = R_2/R_1$, where $R_1 = R_3$ and $R_2 = R_4$, and suppresses high-frequency noise. The capacitor, C_{DC}, decouples the DC content of the second stage. The second stage provides level-shifting through the resistor divider, R_6 and R_7, that are typically made to equal each other so that the sinusoidal sensed signal is centered at 1.5 V, instead of 0 V. If the resistor, R_6, is not bypassed, the second stage can provide additional scaling of the input voltage through the voltage divider established by $\frac{R_6||R_7}{R_5+R_6||R_7}$. The op-amp with unity feedback presents a high input impedance to the level-shifted signal and buffers the output. The diodes, D_1 and D_2, ensure that the output does not exceed the 0 to 3 V band, per ADC's input specifications.

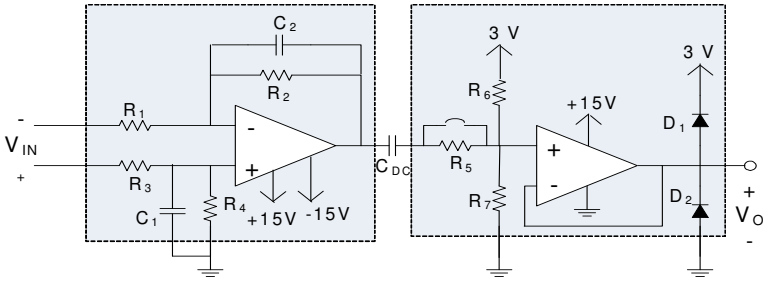


Figure 11.6: Dual-stage signal-conditioning circuit.

Three signal-conditioning circuits are required to condition the voltage and the two current measurements. Texas Instruments TL084 op-amp for the first stage and National Semicondtor's LM2905 op-amp for the second stage are used.

For the main controller, Spectrum Digital's eZdsp evaluation board built around the Texas Instrument's fixed-point TMS320F2812 DSP chip that can operate at a speed of 150 million instructions per second (MIPS) is selected. The DSP chip was designed for motor drive applications and therefore has many useful functionalities

built-in such as up to 16 ADC input channels and up to 16 PWM output channels. The DSP analyzes the sensed waveforms and outputs an ideal PWM signal off a single pin, quadrant information using two pins for specifying current and/or voltage polarity, and a toggle pin that indicates whether the converter should operate in a nominal mode or go into a standby mode when a fault occurs. These three sets of outputs are propagated to the state machine. The DSP also takes in a logic fault signal that is a result of fault outputs from the gate drivers, device temperature monitoring circuit, and control power supply that have been OR'ed together. Once a fault is triggered, the DSP interrupts its normal routine and executes an interrupt request (IRQ) routine.

The program is designed to execute at a rate of 10 kHz, or once every 100 μs, which is the same as the switching period of the converter. The program execution is initiated by the IRQ routine of the ADC, which is triggered at the end of the analog-to-digital conversion of the last channel. The start of conversion itself is initiated by one of the primary timer that is looping at a rate of 10 kHz. The algorithm is summarized as follows:

1. Wait for the ADC interrupt request.

2. While the main routine is waiting for the interrupt to occur, the timer has triggered start-of-conversion in the background. ADC starts converting the measurements. Once all the specified channels have been converted, the ADC interrupt flag is raised.

3. The ADC IRQ routine starts executing as follows:

4. The ADC converter measurements are read from the ADC register.

5. An optional digital low-pass filter can be applied to the measurements.

6. The ADC results are calibrated.

7. The PLL calculates the instantaneous angle, ωt, of the input voltage.

8. ABC-to-DQ0 transformations are applied to the source current three times with references at the fundamental, third and fifth harmonic frequencies. The Q-component of the fundamental, and both the D- and Q-component of the third and fifth harmonics are each driven to zero with an integral compensator. The integral output of the fundamental loop is the constant term in the even harmonic modulation. The outputs of the two sets of integrators for the third and fifth harmonic control loop undergo DQ0-to-ABC transformations with second and fourth harmonic frequencies, respectively, as the references. The results are summed together with the constant term from the fundamental loop and form the ideal duty cycle of the switches.

9. The instantaneous value of the duty is updated on the PWM register.

10. Based on the inductor current polarity, the quadrant information is updated via two GPIO pins.

11. If an external fault is triggered at any time, the associated IRQ routine is executed, subsequently toggling the Standby pin connected with the state machine. In turn, the state machine toggles all the IGBTs to an off state by default.

The PCB design of the controller board is given by Figure 11.7. A 5 V and 3 V linear regulators are built on-board for powering the eZdsp board and level-shifting the measured signals, respectively. A single DSP chip can drive either three-phase, low-voltage D-CAP built with one module per phase, or a single-phase, medium-voltage D-CAP built with two modules per phase; the latter approach is used in the prototype. Sixty-pin headers are designed on both sides of the PCB for passing along both the analog and digital signals between the DSP and up to three modules. The DSP can be mounted on the controller PCB of any one of the three modules.

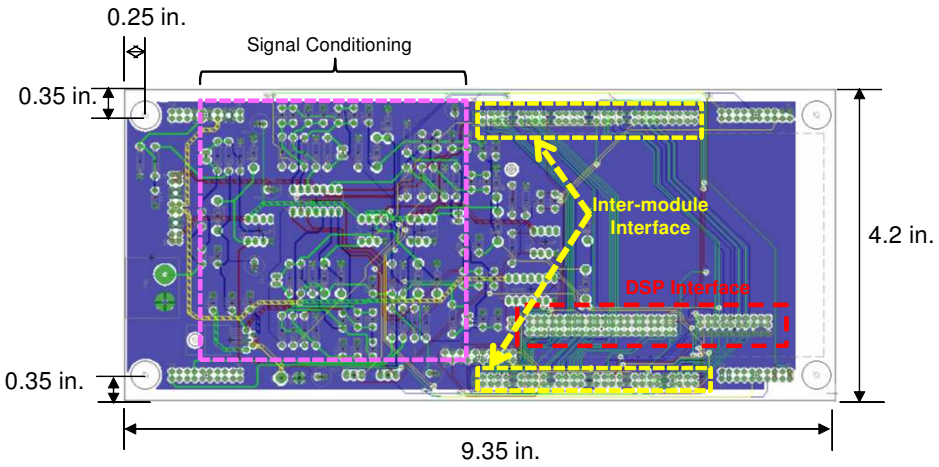


Figure 11.7: PCB design of the signal conditioning and DSP interface board.

11.7 Experimental Results

The final assembled prototype is shown in Figure 11.8. The two modules, various inductors, transformers, capacitors, sensors, and power supply of the D-CAP are mounted onto a standard 19-inch rack. Voltages are measured with Tektronix P5200 differential probes with a 100 MHz bandwidth. The current measurements are made with Tektronix TCP 202 probes with a bandwidth of up to 50 MHz and post-calibration accuracy of ±3 percent. Tektronix oscilloscope TDS5034B with a bandwidth of 350 MHz is used.

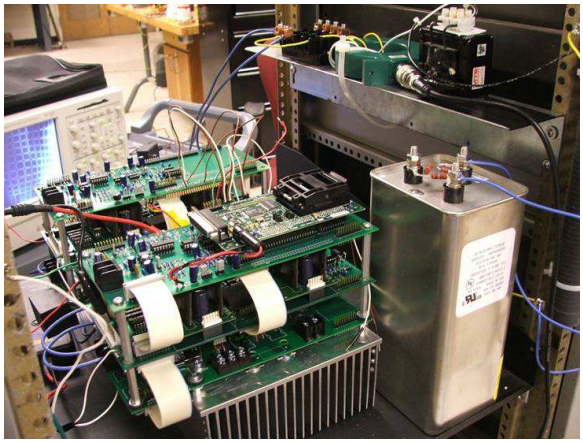


Figure 11.8: A photograph of the experimental setup.

Figure 11.9(a) shows the input line voltage, the unfiltered synthesized voltage imposed across the main capacitor and the series filter inductor, the filtered voltage across the main capacitor, and the inductor current that is flowing through the main capacitor. Figure 11.9(b) shows the voltages across the four snubber capacitors integrated around the IGBTs in the bottom arm of the D-CAP, showing regulation of the half-wave rectified voltage. Figure 11.9(c) shows the voltages across the four IGBTs making up the bottom arm of the D-CAP, which are seen as being equal to each other. Together, these three figures show that despite the inductor current having significant switching harmonics, making it very challenging to determine current polarity accurately around the zero-crossings, the voltage across each of the devices are well behaved, without a single noticeable spike. This is because the AC snubbers not only provides equal voltage sharing between the series-connected devices, but also ensure safe commutation of the devices, even with incorrect commutation sequences due to the controller's inability to assess the polarity of the harmonic-rich inductor current.

Figure 11.10(a) shows the D-CAP is providing power factor correction by bringing the fundamental component of the line current in phase with the line voltage. That the D-CAP is also able to provide harmonic compensation by filtering out the third and the fifth harmonic from the line current is obvious from Figure 11.10(b).

11.8 Conclusions

A buck D-CAP proof-of-concept prototype is designed, built, and tested. The D-CAP prototype is rated to block up to 1.6 kV peak and conduct peak current of up to 50 A. However, due to the limited ratings of the available load banks and the variac in the laboratory, the prototype was tested with approximately 200 V peak input, and 15 A peak capacitor current. The hardware and control implementations are similar to VSI-based active filters except for the requirement for an additional current sensor

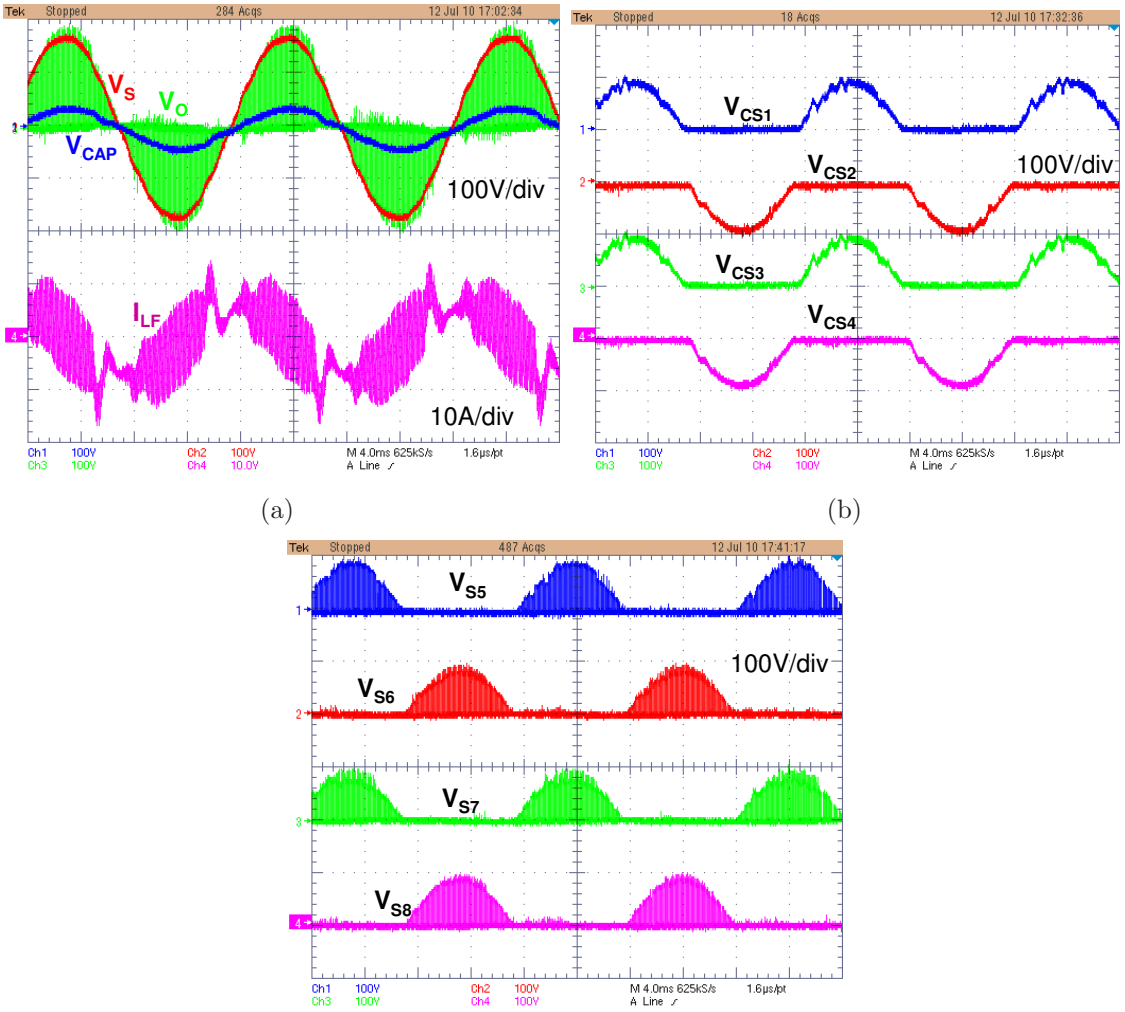
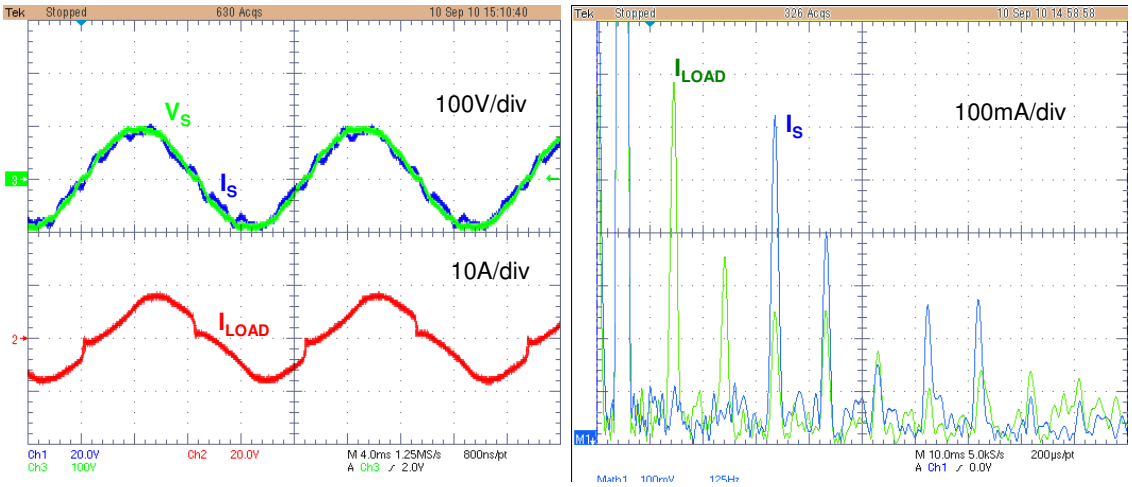


Figure 11.9: Experimental results of the buck D-CAP prototype, where **(a)** the line voltage, V_S, the chopped-up voltage across the passive components, V_O, filtered voltage across the main capacitor, V_{CAP}, and the current through the inductor, I_{LF}, **(b)** voltages across each of the four snubber capacitors of the bottom AC PEBB cell, and **(c)** voltages across each of the four series-connected devices of the bottom AC PEBB cell. These plots demonstrate the effectiveness of the AC snubbers in providing safe commutation and equal voltage sharing.



(a) (b)

Figure 11.10: Experimental results of the buck D-CAP prototype, where **(a)** the line voltage, V_S, line current, I_S, and load current, I_LOAD, demonstrating power factor correction taking place, and **(b)** FFT of the line and load currents demonstrating harmonic filtering of the third and the fifth harmonics.

and a state machine logic circuit to provide current-based multi-step commutation of the AC switches. An EEPROM and a latch were used as a cost-effective means of implementing the state machine in the prototype. Alternatively, an FPGA can also be used instead to implement a more functional state machine. The converter switching frequency of 10 kHz is selected with duty-cycle updates occurring every 100 μs. The multi-step commutation frequency was originally set at 1 MHz, but due to various channel delays and larger than expected rise and fall times of the IGBTs, the frequency is reduced to 800 kHz. The prototype is controlled to supply reactive power and to suppress the third and the fifth harmonics in order to improve the load power factor.

The experimental measurements reveal that the D-CAP is able to provide both dynamic VAR and harmonic compensation quite well. While only the buck topology is implemented, the boost and buck-boost D-CAP topologies are expected to be as effective in their compensation capabilities.

The concept behind the AC snubber is validated via implementation of the low-frequency snubber. The AC snubber enables safe commutation of the devices, fault tolerance of the converter, static and dynamic voltage sharing when series-connecting devices, and spike-free snubber operation. While the fault tolerance was not directly tested, the prototype demonstrated the other three features quite well.

CHAPTER XII

CONCLUSIONS

This work has presented a novel class of Dynamic VAR and Harmonic Compensators (DVHCs), where existing grid assets such as reactors (inductors), condensers (capacitors), and resistors are augmented with a direct AC converter on a single-phase basis to realize a dynamically controllable impedance that can source and sink currents not only at the fundamental line frequency for fulfilling the asset's original functionality, but also at multiple harmonics for active filtering. Since these grid assets already exist on the system, there is only the incremental cost associated with the additional components. But even with a fresh build, the cost is expected to stay low with capacitors and reactors obtainable for $10 to 20 per kVAR and $20 to 30 per kVAR, respectively.

This work has focused on the Dynamic Capacitor (D-CAP), a subclass of the DVHCs, used for dynamically supplying reactive power and providing harmonic filtering. The other subclass of the DVHCs is the Dynamic Inductor (D-IND) for consuming reactive power and providing harmonic filtering. A third type of compensator, Dynamic Resistor (D-RES), is also introduced where a resistor is used to provide harmonic filtering. Each of these three types of compensators can be configured as a buck, boost or a buck-boost, depending on the type of functionality required by the application.

The direct AC converter, as it is converting energy directly from one AC source to another, does not require the use of bulk energy storage elements, thereby obviating the need for electrolytic capacitors and subsequently improving the inherent reliability of the product, widening the operating temperate range, and reducing the burden on

the thermal management system. The grid assets themselves that the converters are interfacing with have already proven to be reliable time and time again over the life of the modern day power system. In order to preserve that reliability, a 'fail-normal' switch comprised of a thyristor-pair is used to bypass the converter, if and when it should fail, reverting back the original functionality of the grid asset.

The voltage blocked by the semiconductor devices in a direct AC converter is the line voltage itself, which is sinusoidal, as opposed to the DC voltage in a VSI. Therefore, for the sinusoidal current of the same magnitude, and depending on the power factor, the switching loss can be slashed by as much as 50 percent when comparing single-phase implementations. In VAR compensators, the fundamental component of the current is always orthogonal to the line voltage, so the conditions for realizing 50 percent reduction in switching losses always exist. That is a significant reduction where switching losses typically constitute more than fifty percent of the overall device losses for a fast switching IGBT. The reduced losses not only simplify the design of the thermal management system, but also cut down on the variable operating costs.

Through the use of latest-generation IGBTs, the technology can respond within 1/10th of a cycle, demonstrating dynamic capabilities at par with the conventional STATCOMs. Unlike the SVCs, the MSCs, and the TSCs, the boost and the buck-boost configurations of the DVHCs can maintain 1 pu of reactive current even when the grid voltage starts to droop. All three configurations, including the buck, are able to dynamically vary their supply of reactive power as required by the system and/or the loads.

The lack of electrolytic capacitors, reduced switching losses, ability to leverage existing grid assets, functionality and performance at par with voltage source inverters, ability to provide unbalanced compensation, modular scalability to medium voltages, and robust designs results in a suite of product solutions that is highly reliable, has low installation and operating costs, small footprint, and versatile and

highly dynamic capabilities for addressing the existing and emerging needs of the current and the future grid. The decreased losses can lead to the designs of the thermal management system that avoid moving elements like fans and pumps, thereby significantly increasing the reliability of the product. The other life-limiting components are the semiconductor devices themselves. Through advancements in silicon carbide and gallium nitride power device technologies, as well as through reduced losses during converter operation, failure modes are expected to decrease and mean-time-to-failure are expected to increase over time.

To understand the characteristics and operation of the DVHCs, this work has developed time-domain models for analyzing the transient and dynamic behavior; frequency-domain models for understanding the steady-state harmonic interactions; and small-signal models for studying the dynamics of the converter due to various perturbations and for extracting transfer functions in designing robust and stable controllers. Control architectures are presented for effectively controlling the D-CAP under high switching frequency. A technique for optimally determining individual commutation angles when using large devices with low switching frequency is also discussed.

In scaling the DVHCs to higher voltages, three transformer-less medium-voltage topologies are presented. They are series-connecting fractionally-rated devices, use of the flying capacitor approach extended to AC voltages, and series cascading two-level cells. These implementations allow direct connect to the medium-voltage grid, obviating the use of transformers, thereby reducing cost, complexity, and footprint. However, because the nature of direct AC converters mandates use of AC or bi-directional switches, complex commutation patterns based on voltage or current polarity are required for coordination. Errors in sensing and processing are bound to exist. If an incorrect commutation pattern is sequenced due to these errors, large spikes that are detrimental to the life of the converter can occur. To address this issue, a novel AC

snubber concept is proposed with two different types of implementations. The AC snubber ensures safe commutation of the switches, provides fault tolerance by managing the energy trapped in parasitics and filters, and enables dynamic and steady-state voltage sharing when integrated around series-connected devices.

Design equations for selecting and rating the devices and components in the buck, the boost, and the buck-boost configurations of the D-CAP are presented. Three sets of example designs, with one at low-voltage and two at medium-voltage, are discussed to demonstrate the typical size and ratings of the various components for operating with a certain set of specifications.

The various models and designs presented in this work have all been validated through either simulation and/or experimental results. The DVHCs, and in particular, the D-CAP have demonstrated stellar performance with dynamic performance comparable to voltage source inverters, but expected reliability, cost, and efficiency better aligned with the SVCs and the TSCs.

12.1 Summary of Contributions

To summarize, this work has made the following contributions:

1. Developed three sets of time-domain models to understand the transient behavior of the D-CAP.

2. Developed small-signal models to understand the converter dynamics, to design controllers, and to assess the stability margins.

3. Developed steady-state frequency-domain models to understand the harmonic interactions between the control handles and the controlled variables in the active filter applications.

4. Developed a strategy for closed-loop control of the DVHCs to provide VAR and harmonic compensation, and single- and three-phase control architectures to

realize it under high switching frequency operation.

5. Applied a previously developed strategy for optimally operating the buck D-CAP when utilizing large power devices with a low switching frequency to the boost and the buck-boost configurations.

6. Developed, designed, and implemented a novel AC snubber concept for realizing safe commutation and fault tolerance in the DVHCs, thereby addressing reliability issues that have plagued direct AC and AC-AC converters.

7. Developed, designed, and implemented approaches to scale the DVHCs to realistic grid voltages, which are beyond the ratings of most off-the-shelf power devices, and presented three example designs for operation up to 13.8 kV.

8. Designed, built, and tested a 40 kVA experimental prototype of the buck D-CAP for providing VAR and harmonic compensation.

12.2 Future Research

This dissertation has presented various types of models for the three configurations of the D-CAP. Similar techniques can be applied to derive the models for the D-RES and the D-IND.

The time-domain models are useful for understanding the transient behavior of the converters. While a closed-form time-continuous analytical models are derived for a constant duty cycle with parasitics and filter elements taken into account, time-discretized expressions had to be utilized for a non-constant duty cycle. Deriving time-continuous solutions to the integro-differential equations for a non-constant duty cycle with parasitics and filter elements accounted would provide a better insight into the temporal relationship between the control variables and the output current.

The frequency-domain models are able to partially address the limitation of the time-domain models by accurately establishing the relationships between the control

variables in the duty cycle and the harmonic components of the injected current. But the frequency-domain models are limited to steady-state operation and cannot be used to accurately model the transient behavior. However, these models can be used to complement the control of the D-CAP by providing a steady-state reference operating point to inject a current with a specific spectral content. A faster responding and converging controller can potentially result from such a control methodology.

The derived linear time-invariant (LTI) small-signal models assist in stability analysis and compensator tuning when the DVHCs are operated with a constant duty cycle for purely fundamental VAR compensation. However, these models are not useful when the converter is controlled with even harmonic modulation for harmonic filtering applications, as the introduction of harmonic terms result in time-variant circuit quantities. Modeling the converter as an LTI system when providing dynamic VAR and harmonic compensation would be highly desirable to analytically tune the linear harmonic controllers, instead of the iterative heuristic approach currently used. Non-linear techniques may also offer an alternative approach to controlling the D-CAP.

The concept behind selective harmonic cultivation (SHC) was presented for optimally controlling the DVHCs when employing large devices operated with a low switching frequency. Due to the dynamic nature of sources and loads on the system, the commutation angles must be tuned in real-time. This factor limits SHC's application due to significant computing resources required by the controller in solving the massively complex non-linear equations. A non-resource-intensive approach to tuning the commutation angles in real-time would be highly desirable. Such an approach would increase market potential for the DVHC systems in high-power applications.

The novel AC snubber concept was presented with two potential implementations. This research implemented the low-frequency version, which is limited by the cost and BIL ratings of the low-frequency snubber transformer when scaling to higher voltages.

The high-frequency DC-DC converter approach has the potential to be much more effective and viable when scaling to medium voltages. Research and development in prototyping the high-frequency AC snubber would be beneficial to validate its potential, which so far has only been gleaned through simulation results.

Lastly, while a small medium-voltage laboratory prototype was implemented, design and development of a 480 V and 13.8 kV D-CAP systems with a reactive power rating of up to 500 kVAR would be beneficial to fully understand the challenges and difficulties in scaling the D-CAP to realistic voltages and power levels. The latent and yet-unobserved weaknesses and limitations of the DVHC system will only start becoming more obvious once the devices and materials are stressed with higher currents and voltages.

APPENDIX A

SELECTIVE HARMONIC CULTIVATION FOR THE BUCK-BOOST D-CAP

A.1 Initilization and Post-Processing

```
clear all;
close all;

Nh = 6;  %% Number of harmonics constrained
Ns = (Nh+2)*2^3;  %% Number of firing angles ,'MaxFunEvals',10000,

% Initialize firing angles and call the fsolve function
a0 = linspace(1e-5,pi*0.99,Ns);
options = optimset('Display','iter','TolX',1e-12);
[a, fval] = fsolve(@myfun_buckboost,a0,options);

%if the outer vectors are outsides the bounds of [0,pi]
while(a(1) < 0 && a(Ns) > pi)
    if(a(1) < 0)
        a = [a(2:Ns) pi];
    end

    if(a(Ns) > pi)
        a = [0 a(1:Ns-1)];
    end

    a0 = a;
    [a, fval] = fsolve(@myfun_buckboost,a0,options);
end
```

```
25
27 %% Convert angles to time and generate switching signals
   t = a/2/pi/60;
29 n = length(t)+2;

31 x(1,1) = 0;
   x(1,2) = 0;
33 x(2*(n-2)+2,1) = 1/60/2;
   x(2*(n-2)+2,2) = 0;
35
   for i=1:n-2
37     x(2*i,1) = t(i);

39     if(i == 1)
           x(2*i,2) = 0;
41     elseif(x(2*(i-1)+1,2) == 0)
           x(2*i,2) = 0;
43     else
           x(2*i,2) = 1;
45     end

47     x(2*i+1,1) = t(i) + 2e-14;

49     if(x(2*i,2) == 1)
           x(2*i+1,2) = 0;
51     else
           x(2*i+1,2) = 1;
53     end

55 end
```

```
if(x(2,1) < 0)
    x(2,1) = 0;
end

if (x(3,1) < 0)
    x(3,1) = 0;
end

% write the switching signals to a variable, x, and file chops.txt
dlmwrite('chops.txt', x, 'delimiter', '\t', ...
          'newline','pc','precision', 15);
type chops.txt

% run Simulink/PowerSim model of the buck-boost converter with firing
% angles specified by x.
sim('DCAP1phase_Harmonic_Elim_buckboost',0.1);
```

A.2 Primary Function

```
function G = myfun_buckboost(a)


    Nh = 6;  %% Number of harmonics constrained
    Ns = (Nh+2)*2^3;  %% Number of firing angles

    %% Define matrix T1
    for m = 1:Nh
        for n = 1:Nh
            A(n,m) = 0;
            B(n,m) = 0;
            C(n,m) = 0;
            D(n,m) = 0;
        end
```

```
    end

15

    for m = 1:Nh
17      for n = 1:Nh
            g = 2*m-1;
19          h = 2*n-1;
            for k = 1:Ns
21              if(g == h)
                    A(n,m) = A(n,m) + (-1)^k*(sin(2*g*a(k))/(2*g)+a(k));
23                  B(n,m) = B(n,m) + (-1)^k*(-cos(2*g*a(k))/(2*g));
                    C(n,m) = C(n,m) + (-1)^k*(-cos(2*g*a(k))/(2*g));
25                  D(n,m) = D(n,m) + (-1)^k*(-sin(2*g*a(k))/(2*g)+a(k))
                        ;
                else
27                  A(n,m) = A(n,m) + (-1)^k*(sin((g+h)*a(k))/(g+h) ...
                        + sin((g-h)*a(k))/(g-h));
29                  B(n,m) = B(n,m) + (-1)^k*(-cos((g+h)*a(k))/(g+h) ...
                        + cos((g-h)*a(k))/(g-h));
31                  C(n,m) = C(n,m) + (-1)^k*(-cos((g+h)*a(k))/(g+h) ...
                        - cos((g-h)*a(k))/(g-h));
33                  D(n,m) = D(n,m) + (-1)^k*(-sin((g+h)*a(k))/(g+h) ...
                        + sin((g-h)*a(k))/(g-h));
35              end
            end
37      end
    end
39

    A = A/pi;
41  B = B/pi;
    C = C/pi;
43  D = D/pi;
    T1 = [A C; B D];
```

```
45
    %% Defining matrix T2
47  for m = 1:Nh
        for n = 1:Nh
49          A(n,m) = 0;
            B(n,m) = 0;
51          C(n,m) = 0;
            D(n,m) = 0;
53      end
    end
55
    for m = 1:Nh
57      for n = 1:Nh
            g = 2*m-1;
59          h = 2*n-1;
            for k = 1:Ns
61              if(g == h)
                    A(n,m) = A(n,m) + (-1)^(k+1)*(sin(2*g*a(k))/(2*g)+a(
                        k));
63                  B(n,m) = B(n,m) + (-1)^(k+1)*(-cos(2*g*a(k))/(2*g));
                    C(n,m) = C(n,m) + (-1)^(k+1)*(-cos(2*g*a(k))/(2*g));
65                  D(n,m) = D(n,m) + (-1)^(k+1)*(-sin(2*g*a(k))/(2*g)+a
                        (k));
                else
67                  A(n,m) = A(n,m) + (-1)^(k+1)*(sin((g+h)*a(k))/(g+h)
                        ...
                        + sin((g-h)*a(k))/(g-h));
69                  B(n,m) = B(n,m) + (-1)^(k+1)*(-cos((g+h)*a(k))/(g+h)
                        ...
                        + cos((g-h)*a(k))/(g-h));
71                  C(n,m) = C(n,m) + (-1)^(k+1)*(-cos((g+h)*a(k))/(g+h)
                        ...
```

```
                        - cos((g-h)*a(k))/(g-h));
73                  D(n,m) = D(n,m) + (-1)^(k+1)*(-sin((g+h)*a(k))/(g+h)
                        ...
                        + sin((g-h)*a(k))/(g-h));
75              end
            end
77
            if(g == h)
79              A(n,m) = A(n,m) + pi;
                D(n,m) = D(n,m) + pi;
81          else
                B(n,m) = B(n,m) + 1/(g+h) - 1/(g-h) - cos((g+h)*pi)/(g+h
                    ) ...
83                  + cos((g-h)*pi)/(g-h);
                C(n,m) = C(n,m) + 1/(g+h) + 1/(g-h) - cos((g+h)*pi)/(g+h
                    ) ...
85                  - cos((g-h)*pi)/(g-h);
            end
87      end
    end
89
    A = A/pi;
91  B = B/pi;
    C = C/pi;
93  D = D/pi;
    T2 = [A C; B D];
95
    %% PFC Capacitor
97
    w = 2*pi*60;
99  Cap = 2.3e-3;
```

```
101     for n = 1:Nh
            h = 2*n-1;
103         zc(n) = 1/(1i*w*h*Cap);
        end
105
        for k = 1:Nh
107         Z11(k,k) = real(zc(k));
            Z12(k,k) = imag(zc(k));
109         Z21(k,k) = -imag(zc(k));
            Z22(k,k) = real(zc(k));
111     end

113     ZC = [Z11 Z12; Z21 Z22];

115     %% R-L Components
        L = 191.2e-6;
117     R = 0.1;

119     for n = 1:Nh
            h = 2*n-1;
121         yrl(n) = 1/(R+1i*w*h*L);
        end
123
        for k = 1:Nh
125         Y11(k,k) = real(yrl(k));
            Y12(k,k) = imag(yrl(k));
127         Y21(k,k) = -imag(yrl(k));
            Y22(k,k) = real(yrl(k));
129     end

131     YRL = [Y11 Y12; Y21 Y22];
```

```
%% Input Third-Order Filter
CF1  = 50e-6;
CF2 = 1.3e-3;
LF1 = 2.2e-6;
RL1 = 0.1;

for n = 1:Nh
    h = 2*n-1;
    f11(n) = 1/(1 + 1i*h*w*RL1*CF2-h^2*w^2*LF1*CF2);
    f12(n) = -(1i*h*w*LF1+RL1)/(1+1i*h*w*RL1*CF2 - h^2*w^2*LF1*CF2);
    f21(n) = 1i*h*w*(CF1+CF2+1i*h*w*RL1*CF1*CF2 - h^2*w^2*LF1*CF1*
        CF2)/(1+1i*h*w*RL1*CF2-h^2*w^2*LF1*CF2);
    f22(n) = 1/(1+1i*h*w*RL1*CF2-h^2*w^2*LF1*CF2);
end

%%Defining Fa11
for k = 1:Nh
    F11_11(k,k) = real(f11(k));
    F11_12(k,k) = imag(f11(k));
    F11_21(k,k) = -imag(f11(k));
    F11_22(k,k) = real(f11(k));
end
F11 = [F11_11 F11_12; F11_21 F11_22];

%%Defining Fa12
for k = 1:Nh
    F12_11(k,k) = real(f12(k));
    F12_12(k,k) = imag(f12(k));
    F12_21(k,k) = -imag(f12(k));
    F12_22(k,k) = real(f12(k));
end
F12 = [F12_11 F12_12; F12_21 F12_22];
```

```
165     %%Defining Fa21
        for k = 1:Nh
167         F21_11(k,k) = real(f21(k));
            F21_12(k,k) = imag(f21(k));
169         F21_21(k,k) = -imag(f21(k));
            F21_22(k,k) = real(f21(k));
171     end
        F21 = [F21_11 F21_12; F21_21 F21_22];
173
        %%Defining Fa22
175     for k = 1:Nh
            F22_11(k,k) = real(f22(k));
177         F22_12(k,k) = imag(f22(k));
            F22_21(k,k) = -imag(f22(k));
179         F22_22(k,k) = real(f22(k));
        end
181     F22 = [F22_11 F22_12; F22_21 F22_22];

183     %% Input Voltage Vector

185     %clear the vectors
        for k = 1:1:2*Nh
187         Vs(k) = 0;
            Is(k) = 0;
189     end

191     %1 to Nh are cosine, Nh+1 to 2Nh are sine terms
        Vs(Nh+1) = 480*sqrt(2/3);
193
        %% Define reference current
195      Is(1) = 450;    % fundamental cosine term
```

```
        Is(2) = 100;     % third harmonic cosine term
197     Is(3) = 0;       % fifth harmonic cosine term
        Is(4) = 100;     % seventh harmonic cosine term
199     Is(5) = 0;       % ninth harmonic cosine term
        Is(6) = 0;       % eleventh harmonic cosine term
201
        Is(Nh+2) = 0;  % third harmonic sine term;
203     Is(Nh+3) = 100; % fifth harmonic sine term;
        Is(Nh+4) = 0;  % seventh harmonic sine term
205     Is(Nh+5) = 50;  % ninth harmonic sine term
        Is(Nh+6) = 0;  % eleventh harmonic sine term
207
      %% Formulate the non-linear equation G
209   Theta_prime = YRL*T2*ZC*T2;
      Theta = eye(length(Theta_prime)) + Theta_prime;
211   G_prime = F12*T1*Theta^-1*YRL*T1;
      G = (F21 + F22*T1*Theta^-1*YRL*T1*(eye(length(G_prime))-G_prime)^-1*
          F11)*Vs'-Is';
213
      %% Generate unconstrained harmoni
215   G(Nh+1) = 0;  %unconstrain the fundamental sine term

217 end
```

REFERENCES

[1] Akagi, H., "Active harmonic filters," *Proceedings of the IEEE*, vol. 93, pp. 2128–2141, Sept-Oct 2005.

[2] Akagi, H., "Modern active filters and traditional passive filters," *Bulletin of the Polish Academy of Sciences - Technical Sciences*, vol. 54, no. 3, pp. 255–269, 2006.

[3] Alakula, M. and Persson, J., "Vector controlled AC/AC converters with a minimum of energy storage," in *Proceed. of International Conference on Power Electronics and Variable-Speed Drives*, pp. 236–239, Oct 1994.

[4] Alexandrovitz, A., Yair, A., and Epstein, E., "Analysis of a static var compensator with optimal energy storage element," *IEEE Transactions on Industrial Electronics*, vol. IE-31, pp. 28–33, Feb 1984.

[5] Baek, J., Yoo, D., and Kim, H., "High-voltage switch using series-connected IGBTs with simple auxiliary circuit," *IEEE Transactions on Industry Applications*, vol. 37, pp. 1832–1839, Nov/Dec 2001.

[6] Belverde, G., Galluzzo, A., Melito, M., Musumeci, S., and Raciti, A., "Active voltage sharing of series connected IGBT devices in bridge applications," in *IEEE Industry Application Society Meeting*, pp. 817–824, October 1998.

[7] Bhattacharya, S., Cheng, P.-T., and Divan, D., "Hybrid solutions for improving passive filter performance in high power applications," *IEEE Transactions on Industry Applications*, vol. 33, pp. 732–747, May/June 1997.

[8] Bhattacharya, S., Divan, D. M., and Banerjee, B., "Active filter implementation," *IEEE Industry Applications Magazine*, vol. 4, pp. 47–63, Sept-Oct. 1988.

[9] Boenig, H. and Cibulka, F., "A static var compensator using a superconducting coil," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-101, pp. 3988–3996, Oct 1982.

[10] Bradshaw, D., "Super reactive power for the power system through Super-VAr/spl trade/ high temperature superconductor dynamic synchronous condensers," in *Conf. Proceed. of 2004 IEEE Power Engineering Society General Meeting*, pp. 2058–2061, June 2004.

[11] Bradshaw, D., "Re: Supervar." E-mail to Anish Prasai, Sept 24, 2011.

[12] Butler, J., "Analysis of factors which influence the application, operation, and design of shunt-capacitor equipments switched in large banks," *Transactions of the American Institute of Electrical Engineers*, vol. 59, no. 12, pp. 795–800, 1940.

[13] Cheng, P.-T., Bhattacharya, S., and Divan, D., "Operation of the dominant active filter under realistic utility conditions," *IEEE Transactions on Industry Applications*, vol. 37, pp. 1037–1044, July-Aug 2001.

[14] Cho, G., Choi, N., Rim, C., and Cho, G., "Modeling, analysis and control of static var compensator using three-level inverter," in *IEEE Industrial Application Society Annual Meeting*, pp. 837–843, 1992.

[15] Consoli, A., Musumeci, S., Oriti, G., and Testa, A., "Active voltage balancement of series connected IGBTs," in *Conf. Proceed. of IEEE Industry Applications Conference*, pp. 2752–2758, Oct 1995.

[16] Corzine, K. and Familiant, Y., "A new cascaded multilevel H-bridge drive," *IEEE Transactions on Power Electronics*, vol. 17, pp. 125–131, Jan 2002.

[17] Cox, M. and Mirbod, A., "A new static var compensator for an arc furnace," *IEEE Transactions on Power Systems*, vol. 1, pp. 110–119, Aug 1986.

[18] Divan, D., "Nondissipative switched networks for high-power applications," *Electronics Letters*, vol. 20, pp. 277–279, March 1984.

[19] Divan, D. and Sastry, J., "Inverter-less active filters - A new concept in harmonic and var compensation," in *Conf. Proc. Of IEEE PESC 2007*, pp. 2926–2932, June 2007.

[20] Divan, D. and Sastry, J., "Controllable Network Transformers," in *Conf. Proceed. of IEEE Power Electronics Specialists Conference*, pp. 2340–2345, June 2008.

[21] Divan, D. and Sastry, J., "Inverter-less STATCOMs," in *Conf. Proceed. of IEEE Power Electronics Specialists Conference*, pp. 1372–1377, June 2008.

[22] Divan, D. and Sastry, J., "Control of multilevel direct AC converters," in *Conf. Proceed. of IEEE Energy Conversion Congress and Exposition*, pp. 3077–3084, Sept 2009.

[23] Divan, D. M., Bhattacharya, S., and Banerjee, B., "Synchronous frame harmonic isolator using active series filter," in *Conf. Proc. Of EPE*, pp. 30–35, 1991.

[24] Divan, D. and Sastry, J., "Voltage synthesis using virtual quadrature sources - a new concept in AC power conversion," *IEEE Transactions on Power Electronics*, vol. 23, pp. 3004–3013, Nov. 2008.

[25] Electronic Concepts, "UL30 series Unlytic." http://www.ecicaps.com, Sept 2011.

[26] Federal Energy Regulatory Commission, *Principles for Efficient and Reliable Reactive Power Supply and Consumption*, docket no. ad05-1-000 ed., February 2005.

[27] Filho, R. S., Seixas, P., Cortizo, P., Torres, L., and Souza, A., "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Transactions on Industrial Electronics*, vol. 55, pp. 2923–2932, Aug. 2008.

[28] Funkhouser, A., Sickle, R. V., and Shankle, D., "Switching high-voltage shunt capacitor banks," *Transactions of the American Institute of Electrical Engineers*, vol. 70, no. 1, pp. 129–137, 1951.

[29] Gao, F. and Iravani, M., "Dynamic model of a space vector modulated matrix converter," *IEEE Transactions on Power Delivery*, vol. 22, pp. 1696–1705, July 2007.

[30] Gasperi, M., "Life prediction modeling of bus capacitors in AC variable frequency drives," *IEEE Transactions on Industry Applications*, vol. 41, pp. 1430–1435, Nov.-Dec. 2005.

[31] Gyugyi, L., "Power electronics in electric utilities: static var compensators," *Proceedings of the IEEE*, vol. 76, pp. 483–494, April 1988.

[32] Haga, H., Ohishi, K., and Ando, I., "Development of economical UPS system having active filter across DC-bus," in *Proceed. of European Conference on Power Electronics and Applications*, pp. 1–10, August 2006.

[33] Hong, S., Chitta, V., and Torrey, D., "Series connection of IGBTs with active voltage balancing," *IEEE Transactions on Industry Applications*, vol. 35, pp. 917–923, July/August 1999.

[34] Hopkins, D. and Pellissier, P., "A high-voltage electrolytic capacitor bank," *IRE Transactions on Nuclear Science*, vol. 9, pp. 68–73, April 1962.

[35] Hosono, I., Yano, M., Takeda, M., Yuya, S., and Sueda, S., "Suppression and measurement of arc furnace flicker with a large static var compensator," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-98, pp. 2276–2284, Nov/Dec 1979.

[36] Imam, A., Divan, D., Harley, R., and Habetlar, T., "Electrolytic capacitor failure mechanism due to inrush current," in *Proceed. of IEEE Industry Applications Conference 2007*, pp. 730–736, Sept. 2007.

[37] Issouribehere, P., Issouribehere, F., Barbera, G., and Gomez, D., "Measurements and studies of harmonics and switching, transients in large hv shunt capacitor banks," in *IEEE Power Engineering Society General Meeting*, pp. 1–8, 2007.

[38] Jang, S., Ahn, S., Ryoo, H., and Rim, G., "A comparative study of the gate driver circuits for series stacking of semiconductor switches," in *Conf. Proceed. of 2010 IEEE International Power Modulator and High Voltage Conference*, pp. 322–326, May 2010.

[39] Jin, H., Goos, G., and Lopez, L., "An efficient switched-reactor-based static var compensator," *IEEE Transactions on Industry Applications*, vol. 30, pp. 998–1005, July-Aug 1994.

[40] Johns, G., "Analyzing the potential impact of low-cost compact fluorescent lamps on a rural distribution system in the Tennesse Valley Authority service territory," Master's thesis, Tennessee Technological University, Cookeville, TN, Dec. 2009.

[41] Kojori, H., Dewan, S., and Lavers, J., "A large-scale PWM solid-state synchronous condenser," *IEEE Transactions on Industrial Application*, vol. 28, pp. 41–49, Jan/Feb 1992.

[42] Kolar, J., Schafmeister, F., Round, S., and Ertl, H., "Novel three-phase AC-AC sparse matrix converters," *IEEE Transactions on Power Electronics*, vol. 22, pp. 1649–1661, Sept. 2007.

[43] Kueck, J., Kirby, B., Rizy, T., Li, F., and Fall, N., "Reactive power from distributed energy," *The Electricity Journal*, vol. 19, pp. 27–38, December 2006.

[44] Kwak, S. and Toliyat, H., "An approach to fault-tolerant three-phase matrix converter drives," *IEEE Transactions on Energy Conversion*, vol. 22, pp. 855–863, Dec. 2007.

[45] Lee, F., "Modeling and control of converters." ECE5254 Class Notes from Virginia Tech, Aug-Dec 2004.

[46] Lee, K., Jahns, T., Venkataramanan, G., and Berkopec, W., "DC-bus electrolytic capacitor stress in adjustable-speed drives under input voltage unbalance and sag conditions," *IEEE Transactions on Industry Applications*, vol. 43, pp. 495–504, March-April 2007.

[47] Lezana, P., Rodriguez, J., and Oyarzun, D., "Cascaded multilevel inverter with regeneration capability and reduced number of switches," *IEEE Transactions on Industrial Electronics*, vol. 55, pp. 1059–1066, March 2008.

[48] Li, F., Kueck, J., Rizy, T., and King, T., "A preliminary analysis of the economics of using distributed energy as a source of reactive power supply," Tech. Rep. ORNL/TM-2006/014, Oak Ridge National Laboratory, April 2006.

[49] Liu, Y., Hong, H., and Huang, A., "Real-time calculation of switching angles minimizing THD for multilevel inverters with step modulation," *IEEE Transactions on Industrial Electronics*, vol. 56, pp. 285–293, Feb 2009.

[50] Loh, P., Blaabjerg, F., Gao, F., Baby, A., and Tan, D., "Pulsewidth modulation of neutral-point-clamped indirect matrix converter," *IEEE Transactions on Industry Applications*, vol. 44, pp. 1805–1814, Nov.-Dec. 2008.

[51] Makram, E., Subramaniam, E., Girgis, A., and Catoe, R., "Harmonic filter design using actual recorded data," *IEEE Transactions on Industry Applications*, vol. 29, pp. 1176–1183, Nov/Dec 1993.

[52] Marchesoni, M. and Tenca, P., "Diode-clamped multilevel converters: a practicable way to balance DC-link voltages," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 752–765, Aug 2002.

[53] McGrath, B., Meynard, T., Gateau, G., and Holmes, D., "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," *IEEE Transactions on Power Electronics*, vol. 22, pp. 508–516, March 2007.

[54] Miller, D., "Application guide for shunt capacitors on industrial distribution system at medium voltage levels," *IEEE Transactions on Industry Applications*, vol. IA-12, pp. 444–459, Sept 1976.

[55] Mishra, M., Joshi, A., and Ghosh, A., "Control schemes for equalization of capacitor voltages in neutral clamped shunt compensator," *IEEE Transactions on Power Delivery*, vol. 18, pp. 538–544, April 2003.

[56] Moore, P. and Portugues, I., "The influence of personal computer processing modes on line current harmonics," *IEEE Transactions on Power Delivery*, vol. 18, pp. 1363–1368, Oct 2003.

[57] Moran, L., Ziogas, P., and Joos, G., "Analysis and design of a three-phase synchronous solid-state var compensator," *IEEE Transactions on Industrial Application*, vol. 25, pp. 598–608, July/Aug 1989.

[58] Musunuri, S. and Dehnavi, G., "Comparison of STATCOM, SVC, TCSC, and SSSC performance in steady-state voltage stability improvement," in *Conf. Proceed. of 2010 North American Power Symposium (NAPS)*, pp. 1–7, Sept. 2010.

[59] Neft, C., "AC power supplied static switching apparatus having energy recovery capability." US Patent 4697230, 1986.

[60] Nguyen, M., Jung, Y., Lim, Y., and Kim, Y., "A single-phase Z-source buck-boost matrix converter," *IEEE Transactions on Power Electronics*, vol. 25, pp. 453–462, Feb 2010.

[61] Nielsen, P., Blaabjerg, F., and Pedersen, J., "New protection issues of matrix converter: Design considerations for adjustable-speed drives," *IEEE Transactions on Industry Applications*, vol. 35, pp. 1150–1161, Sept/Oct 1999.

[62] Noroozian, M., Pertersson, A. N., Thorvaldson, B., Nilsson, B. A., and Taylor, C. W., "Benefits of SVC and STATCOM for electric utility application," in *Proc. Of IEEE PES Transmission and Distribution Conference and Exposition 2003*, pp. 1192–1199, 2003.

[63] Palmer, P. and Githiari, A., "The series connection of IGBTs with active voltage sharing," *IEEE Transactions on Power Electronics*, vol. 12, pp. 637–644, July 1997.

[64] Palmer, P., Rajamani, H., and Dutton, N., "Experimental comparison of methods of employing IGBTs connected in series," *IEE Proceedings - Electrical Power Application*, vol. 151, pp. 576–582, Sept. 2004.

[65] Patel, H. and Hoft, R., "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part I-Harmonic elimination," *IEEE Transactions on Industry Applications*, vol. 1A-9, pp. 310–317, May 1973.

[66] Prasai, A. and Divan, D., "Zero-Energy Sag Correctors - optimizing dynamic voltage restorers for industrial applications," *IEEE Transactions on Industry Applications*, vol. 44, pp. 1777–1784, Nov.-Dec. 2008.

[67] Prasai, A., Sastry, J., and Divan, D., "Dynamic Capacitor (D-CAP): An integrated approach to reactive and harmonic compensation," *IEEE Transactions on Industry Applications*, vol. 46, pp. 2518–2525, Nov/Dec 2010.

[68] Rice, D., "Adjustable speed drive and power rectifier harmonics-their effect on power systems components," *IEEE Transactions on Industry Applications*, vol. IA-22, pp. 161–177, Jan. 1986.

[69] Ristow, A., Begovic, M., Pregelj, A., and Rohatgi, A., "Development of a methodology for improving photovoltaic inverter reliability," *IEEE Transactions on Industrial Electronics*, vol. 55, pp. 2581–2592, July 2008.

[70] Rodriguez, J., Lai, J., and Peng, F., "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 724–738, Aug 2002.

[71] Rogers, D., Divan, D., and Green, T., "Modelling and optimal switching pattern generation for AC to AC power converters," in *Conf. Proceed. of 2010 IEEE Power and Energy Society General Meeting*, pp. 1–8, July 2010.

[72] Santoso, S., "On determining the relative location of switched capacitor banks," *IEEE Transactions on Power Delivery*, vol. 22, pp. 1108–1116, April 2007.

[73] Sasagawa, K., Abe, Y., and Matsuse, K., "Voltage-balancing method for IGBTs connected in series," *IEEE Transactions on Industry Applications*, vol. 40, pp. 1025–1030, July/August 2004.

[74] Sastry, J., *Direct AC Control of Grid Assets*. PhD thesis, Georgia Institute of Technology, August 2011.

[75] Schatz, J., "Re: Harmonic filtering at the distribution level." E-mail to Anish Prasai, November 8, 2011.

[76] Schonberger, J., "A single phase multi-string PV inverter with minimal bus capacitance," in *Proceed. of 13th European Conference on Power Electronics And Applications*, pp. 1–10, Sept. 2009.

[77] Schroeder, T. and Bloomquist, W., "Automatic control and switching equipment for capacitor banks and its application," *Transactions of the American Institute of Electrical Engineers*, vol. 63, no. 9, pp. 649–654, 1944.

[78] Shi, Y., Yang, X., He, Q., and Wang, Z., "Research on a novel capacitor clamped multilevel matrix converter," *IEEE Transactions on Power Electronics*, vol. 20, pp. 1055–1065, Sept. 2005.

[79] Silva, S., Lopes, B., Filho, B., Campana, R., and Bosventura, W., "Performance evaluation of PLL algorithms for single-phase grid-connected systems," in *Conference Proceedings of IEEE Industry Application Conference*, pp. 2259–2263, Oct 2004.

[80] Singh, B., Saha, R., Chandra, A., and Al-Haddad, K., "Static synchronous compensators (STATCOM): A review," *IET Power Electronics*, vol. 2, pp. 297–324, July 2009.

[81] Sode-Yome, A., Mithulananthan, N., and Lee, K., "A comprehensive comparison of FACTS devices for enhancing static voltage stability," in *Conf. Proceed. of IEEE Power Engineering Society General Meeting*, pp. 1–8, June 2007.

[82] Sun, J., Beineke, S., and Grotstollen, H., "Optimal PWM based on real-time solution of harmonic elimination equations," *IEEE Transactions on Power Electronics*, vol. 11, pp. 612–621, Jul 1996.

[83] U.S. Department of Energy, "States with Renewable Portfolio Standards." `http://apps1.eere.energy.gov/states/maps/renewable_portfolio_states.cfm`, May 2009.

[84] Vodyakho, O. and Mi, C., "Three-level inverter-based shunt active power filter in three-phase three-wire and four-wire systems," *IEEE Transactions on Power Electronics*, vol. 24, pp. 1350–1363, May 2009.

[85] Wang, J., Ahmadi, D., and Wang, R., "Optimal PWM method based on harmonics injection and equal area criteria," in *Conf. Proceed. of IEEE Energy Conversion Congress and Exposition*, pp. 1439–1443, Sept. 2009.

[86] Weedy, B., *Electric Power Systems*. John Wiley and Sons Ltd, 2nd ed., 1972.

[87] Wheeler, P., Clare, J., Empringham, L., Bland, M., and Kerris, K., "Matrix converters," *IEEE Industry Applications Magazine*, vol. 10, pp. 59–65, Jan-Feb 2004.

[88] Wheeler, P., Rodriguez, J., Clare, J., Empringham, L., and Weinstein, A., "Matrix converters: A technology review," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 276–288, April 2002.

[89] Xiaomin, K., Corzine, K., and Familiant, Y., "A unique fault-tolerant design for flying capacitor multilevel inverter," *IEEE Transactions on Power Electronics*, vol. 19, pp. 979–987, July 2004.

[90] Yong, J., Chen, L., Nassif, A., and Xu, W., "A frequency-domain harmonic model for compact fluorescent lamps," *IEEE Transactions on Power Delivery*, vol. 25, pp. 1182–1189, April 2010.

VITA

Anish Prasai was born in the small, mountainous country of Nepal in a chilly December night in 1981. He moved with his family to the State of Virginia when he was a small boy. The author's attraction to engineering was made apparent at an early age when he was observed breaking open his toys in order to figure out how they functioned. It was not until much later that he eventually figured out how to put them back together in a working order again.

The author's affinity towards Electrical Engineering developed academically in the latter half of his high school years. Upon matriculating into Virginia Tech in the Fall of 2000, his attraction towards the field was at a full bloom. The author completed his B.S. degree in Electrical Engineering in the Spring of 2004 with specialization in the field of power electronics. He decided to continue his studies towards a Master's degree in Electrical Engineering in the Fall of 2004 with the Center for Power Electronics System (CPES) at Virginia Tech under Professor Willem G. Odendaal, graduating a couple years later in the Summer of 2006.

To further his graduate study in power electronics and obtain a PhD degree in Electrical Engineering, he enrolled at Georgia Tech under the supervision of Professor M. Divan. Under Professor Divan, the author was able to hone his skill sets further and expand his knowledge base in the field of power electronics and power systems.